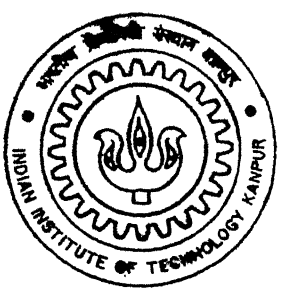
IMPROVED UTILITY INTERFACE FOR AC DRIVE SYSTEM WITH VOLTAGE SAG RIDE-THROUGH CAPABILITY

By

Pankaj Jaiswal



DEPARTMENT OF ELECTRICAL ENGINEERING

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A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Technology

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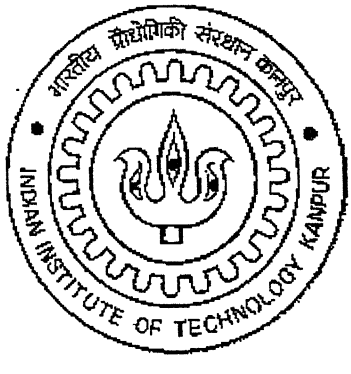

Department of Electrical Engineering
INDIAN INSTITUTE OF TECHNOLOGY, KANPUR
May, 2003

CERTIFICATE

This is certified that the work contained in this thesis entitled **"Improved Utility Interface for ac Drive System with Voltage Sag Ride-Through Capability"**, by Pankaj Jaiswal, has been carried out under our supervision and that this work has not been submitted elsewhere for any degree.

09/5/03

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Abstract

Voltage Sags are of common occurrence even in most advanced power system networks. In voltage sensitive applications like textile and paper mills, even brief voltage sag may potentially cause an Adjustable Speed Drive (ASD) to introduce speed fluctuations, which damage the end product, or may also cause a tripping resulting in heavy losses. Further, as the harmonic restrictions are becoming stricter, the front end converter used in ASD to get a dc power from ac supply needs to be controlled to draw nearly sinusoidal current. Hence an improved utility interface is required that can draw almost sinusoidal current at unity power factor from supply, keep the dc link voltage constant under varying supply voltage conditions and allow bi-directional power flow making regenerative operation possible.

In this dissertation, an advanced converter called Synchronous Link Converter (SLC) has been used as the front end converter for ac drive system. Indirect current control scheme has been used with constant switching frequency pulse width modulation, drawing nearly sinusoidal (low in harmonics) current at unity power factor from the supply. With this closed loop control scheme, the dc link voltage is maintained close to the reference value in voltage sag as well as swell conditions, thus providing the ac drive with voltage sag ride-through capability. By de-rating the front end converter, the maximum sag that it can ride-through can be increased. Further, at lower loads a higher sag can be compensated. The performance evaluation of this advanced utility interface for ac drive systems has been done by simulation studies in SABER simulator. A laboratory prototype has been fabricated and tested successfully. The real

time control algorithm has been implemented using a PC (Pentium) with PCL-208 data acquisition card.

Key words

Synchronous link converter (SLC), unity power factor, Adjustable Speed Drives (ASD), front end converter, SABER simulator, PC based implementation, regenerative operation.

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Pankaj

Dedicated
to my
beloved parents
and Sisters

Contents

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List of Symbols

L_s	Synchronous Link Reactance
X_L	Synchronous Link Inductor Reactance
C	Capacitance of the dc link capacitor
V_c	r.m.s. phasor of Converter Input Voltage
V_{dc}	dc Link Voltage
V_s	Source Voltage
V_{c1}	Fundamental Component of Converter Input Voltage
δ	Angle Between Phasors V_{c1} and V_s
I_s	Input supply current for single phase
I_{s1}	r.m.s. Phasor of Fundamental Component of source current for single phase
V_L	Voltage Drop across Synchronous Link Inductor
vs	Instantaneous supply voltage
vc	Instantaneous converter input voltage
vdc	Instantaneous dc link voltage
ω	Angular frequency of the supply voltage
P	Power transferred from source to converter
M_f	Modulation index for pulse width modulation
I_d	The current supplied by the SLC to dc link
$M_{f\,max}$	Maximum modulation index
f_{sw}	Switching frequency
V_{ch}	h^{th} harmonic component in the V_c
vr	R phase voltage of the three phase supply
vy	Y phase voltage of the three phase supply
vb	B phase voltage of the three phase supply
V_{ll}	Line to line voltage of the three phase voltage
sag	Voltage sag magnitude in per unit
η_{inv}	Efficiency of the load side inverter p.u.
η_{SLC}	Efficiency of the SLC in p.u.

Chapter 1

Introduction

1.1 Background

Voltage Sags are of common occurrence in supply system all over the world. It is defined as the fall in rms value of voltage for a small period of time ranging from half a cycle to 150 cycles or even up to one minute. It is caused by the faults in the plant or power system, motor starting, fast re-closing of circuit breakers. Sags are considered severe when they are more than 12%, i.e. the fall in the magnitude of voltage is more than 12% of the nominal voltage.

Surveys report, voltage sags are the main cause of plant disturbances. For example in a survey [1] it has been reported that 68% of the disturbances reported were voltage sags and were the only cause of production loss. This loss was caused by voltage drops more than 13% of rated voltage and duration of more than 8.3 ms (half

cycle). Another survey [2] states that a little more than 62% of the disturbances recorded were voltage sags with duration of less than half a second (30 cycles). In another study [3] conducted by Bell Telephone Laboratories, voltage sags accounted for 87.2% of measured events. In this survey the average sag duration was 190 ms (11.4 cycles) and none occurred for less than 100 ms (6 cycles).

Another study [3] in Mexico gives the average sag duration to be 17.8 cycles. It also says that the disturbances that caused voltage sags in the range of 20%-30% of rated voltage are more than those in the range of 10%-20% and these in turn are above those in the range 0%-10%. This study also shows that voltage sag with duration 12 cycles or more and having voltage drop of more than 20% cause an outage in the continuous process. However, most of the voltage sags are within 40% of nominal voltage.

1.2 Voltage Sag and Adjustable Speed Drives (ASD's)

The application of ASD's in commercial and industrial facilities is increasing due to improved efficiency, energy savings, and process control. However, ASD's are often susceptible to voltage disturbances, such as sags, swells, transients (e.g., due to capacitor switching), and momentary interruptions (outages). The problem of voltage sags is of importance because it can cause loss of production and revenue due to the tripping of equipment sensitive to voltage variations. In textile and paper mills, small voltage sag may potentially cause an Adjustable Speed Drive (ASD) to introduce speed fluctuations which damage the end product. Furthermore, small voltage sag may also

cause a momentary decrease in dc link voltage, triggering an under voltage trip or resulting in an over-current trip.

Depending on the application, and the characteristics of the disturbance, the ASD-controlled process may be momentarily interrupted or permanently tripped out. This can result in a significant loss in revenue and costly downtime. For example, in continuous process systems, such as metal casters, paper machines, winders, extruders, etc., any interruptions to that process can halt the entire manufacturing flow, with extremely costly implications. The cumulative cost estimates of power disturbances in the U.S. range from $20 000 000 000 to $100 000 000 000 per year [4], where industries have reported losses ranging from $10 000 to $1 000 000 per disrupting event. These losses can be significantly reduced for *critical production processes* by using ASD's with ride-through capabilities.

1.3 Objectives of the Thesis

The objectives of the present work are to provide voltage sag ride through as well as under voltage operation capability to an adjustable speed drive system, drawing nearly sinusoidal current (almost free from harmonics) from the supply at unity power factor (u.p.f.), also allowing power flow in both the directions, so that in case of regeneration, power can be returned to supply, thus, increasing the efficiency of the drive. It uses either a single phase or three phase Synchronous Link Converter (SLC). The dc link voltage is maintained constant by a closed loop control. u.p.f. condition at the utility interface is obtained by indirect current control of SLC.

The present thesis deals with design, digital simulation (using SABER simulator) and PC based implementation of the topology with the above mentioned features. It is called a Utility friendly drive system with voltage sag ride through capability because it operates at the condition which is best for the utility, i.e., at unity power factor and sinusoidal current, and has regenerative capability.

1.5 Organization of the Thesis

In chapter 2 of this thesis a status review of Voltage Sag and its consequences on Adjustable Speed Drives have been given. The different approaches and methodologies that are being used and being developed to deal with the Voltage Sag problem have been discussed.

Chapter 3 gives the details of the Synchronous Link Converter, its operating principle, design criteria and control strategy, and its application as the front-end converter for Adjustable Speed Drives. Detailed simulation studies have been given to show the performance of the proposed topology.

In chapter 4 the details of practical implementation of the proposed SLC with the indirect current control strategy have been given. A comparison of experimental and simulation results of similar designs has been given.

In chapter 5 the contributions of the present thesis work have been enumerated along with the suggestions for future work.

Chapter 2

Voltage Sag and Adjustable Speed Drives – A Status Review

2.1 Introduction

With today's advanced control strategies, the Adjustable Speed Drives are being accepted in commercial and industrial facilities. That is why voltage sag ride through capability is being emphasized more and more. Several methods have been tried to get the ride through capability.

To reduce nuisance tripping of ASD's equipment with capacitor switching transients, utility voltage sag and under voltage, it is often suggested to add 3%–5% line input reactors in series. It has been shown in literature [5] that with the additional line reactance, the dc-link voltage variation is larger under voltage sag and can aggravate the

nuisance tripping issue. Thus, adding a line reactor in front of ASD equipment does not help the effects of voltage sags, but does reduce harmonic currents in the ac supply and the diode peak current.

There are two main reasons for tripping of ASD's because of voltage sag. The first is that the power supply for the control electronics of the drive also experiences a voltage sag. If the power supply cannot sustain adequate voltage for the control electronics, the drive has to be shut down as a safety measure against losing control of the drive. When providing ride-through capability for an ASD, it is necessary to equip the drive with a power supply for the control electronics, which is able to withstand the maximum sag the drive is rated for.

The second reason is that some processes cannot tolerate the loss of precise speed or torque control, even for a few seconds. For inverters under current regulation, the current regulator can saturate if the dc-bus voltage drops to a very low value. For a motor under a standard volts-per-hertz control, if the dc-bus voltage drops to a very low value, the drive may not be able to deliver the required voltage to the motor at a certain speed. The dc-bus voltage therefore needs to be kept within reasonable bounds from the nominal dc-bus voltage during a sag.

2.2 Voltage Sag Ride-through for Adjustable Speed Drives

Several methods have been proposed in the literature to prevent ASD's from tripping as a result of voltage sags. These can be classified into three categories: (1)

installation of compensating equipment; (2) an alternate power supply; and (3) drive topology modifications.

A. Compensating Equipment

Dynamic voltage support can be provided in the distribution system by installing a dynamic voltage restorer or static compensator (STATCOM). Within the plant, an active power line conditioner can be used. These devices need to be equipped with energy storage in order to compensate for voltage sags. The amount of stored energy determines the magnitude and duration of sags for which ride-through can be provided. Energy storage devices are expensive, and a tradeoff between ride-through capability and cost is required.

B. Alternate Power Supply

A separate feeder can isolate the plant from the rest of the power system, but this is a very costly solution. In the plant, sensitive equipment can be isolated from the main supply through an on-line uninterruptible power supply (UPS). Disadvantages related to the use of a UPS include the cost of the UPS, especially at high power levels, and the losses associated with the UPS, which reduce the efficiency of the system. Usually, batteries are used for energy storage in the UPS, but they require regular maintenance and can take up a significant amount of floor space, depending on the amount of ride-through which is provided. The number of discharge cycles the batteries can stand is also limited.

C. Topologies with Storage Facilities

It is possible to obtain a backup energy storage system designed specifically for the short duration events that occur in the system like voltage sags, transients etc. A variety of energy storage technologies are candidates for providing the needed full-power ASD ride-through. Most of the present-day UPS designs are based on 5, 10, or 15 min of backup supply. Several different mediums, including the following, can be used to store the energy required by the sensitive loads [4], [6]:

1) Superconducting magnetic coils;

2) Capacitors;

3) Batteries;

4) Rotating inertia.

These Systems have been used pretty effectively for ride through of voltage sag condition these can ride through even for voltage interruptions. These have limitations of being costly, bulky, space consuming, requiring maintenance and inability to solve the problem of under voltage which is a frequent happening in developing countries like ours.

D. Drive Topology Modifications

In order to achieve voltage sag ride-through, the modifications to the drive have to regulate the dc-bus voltage to within reasonable bounds from the nominal dc-bus voltage. It also has to be ensured that sufficient voltage is provided to the ASD control electronics during the sag. Commercial power supplies capable of operating at reduced voltage are

available and, therefore, now the focus is on the dc-bus voltage regulation requirement. The Fig. 2.1 below shows a typical topology of ASD.

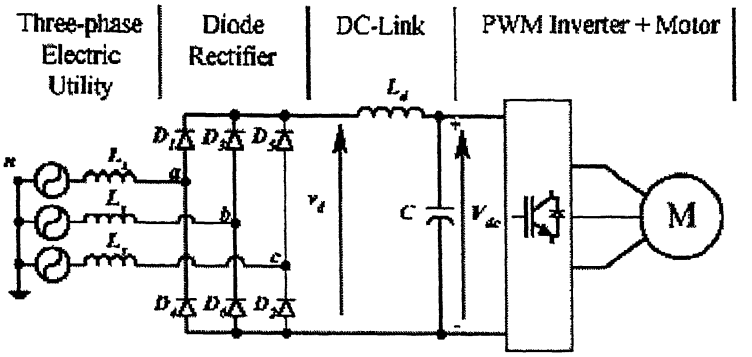


Fig. 2.1- Typical ASD topology

There are several approaches to topological modifications of ASD's:

i) Based on harmonic pollution: With the increased use of microelectronic and power electronic systems the harmonic pollution in the system has been increased a lot. Therefore, the harmonic restrictions imposed by the utilities have become very strict. So, one approach is to reduce harmonics by topological modifications. Whereas the other approach is to use the least cost topology even though it is generating harmonics.

ii) Based on loading: When voltage sag occurs in the system, it occurs due to some fault or overloading. At that time, in certain applications, we can make up for the voltage sag by drawing higher current (constant power). This loads the utility further. So, one approach is to avoid drawing higher current from the utility and making up for the sag by taking power from some kind of storage system. There are several storage systems like adding more capacitors, use of load inertia, flywheel, battery back-up systems, SMES system etc. These systems can ride through even in case of voltage interruptions. But

such storage systems are costly, require space and are unable to supply power continuously i.e. they can not run in under voltage condition. Therefore, the other approach is to use a topology that increases the load on the utility but keeps the dc link voltage constant.

Different Topologies:

1) Boost Converter: A boost converter can be added between the rectifier and dc-link capacitors, as shown in Fig. 2.2. Under sag conditions, the boost converter will regulate the dc bus voltage to the minimum dc-bus voltage required by the inverter.

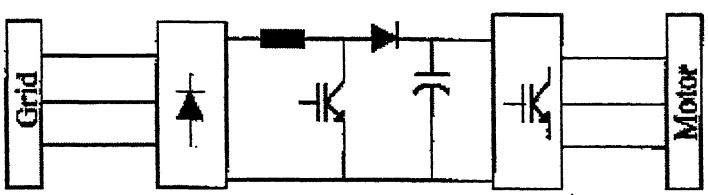


Fig. 2.2- ASD with boost converter added to the dc bus

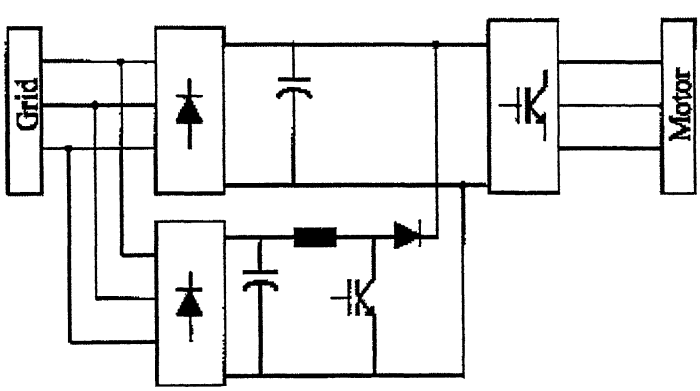


Fig. 2.3 ASD with ride through unit added in parallel to the rectifier

Additional components, as well as control hardware, are required, and the rectifier and boost converter components have to be de-rated. For example, if the drive is rated to ride through a 50% sag, the rectifier and boost converter devices have to be de-rated by a factor of two. Energy storage can be added to increase the ride-through capability of the drive. For retrofit applications, a rectifier and boost converter can be added in parallel to the rectifier, as shown in Fig. 2.3. When a sag occurs, the load power is processed through this parallel unit, with the boost converter regulating the dc bus voltage.

*2) **Advanced Utility Interface:*** An advanced utility interface, where the diode rectifier is replaced by an active rectifier, as shown in Fig. 2.4, can provide an ASD with voltage sag ride-through. Active rectifier front ends to drives are becoming more common because some loads require bidirectional power flow for four quadrant operation of the drive, also diode bridge rectifiers cause harmonic pollution in the power system. As awareness of the adverse effects of harmonics on transformers and other power system equipments grows, more diode bridges will be replaced by active rectifiers. Where an active rectifier has already been decided on, due to the above-mentioned considerations, voltage sag ride-through capability can be incorporated by an appropriate dc-bus voltage regulation strategy and, if necessary, de-rating of the rectifier. The increased process reliability achieved by installing ASD's with voltage sag ride-through may well become another factor driving

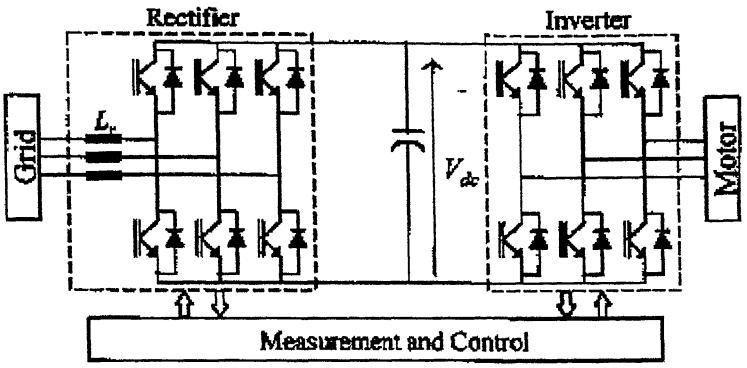


Fig. 2.4 ASD with active rectifier front end

the market for active rectifiers in drives. The range of sags for which ride-through can be provided is limited by the current rating of the rectifier, but there is no limit on the duration of sags. By de-rating the rectifier, the ride-through capability can be increased rather it can work in under voltage condition. Since the thermal rating of a the semiconductor devices allows for over-currents for a certain duration, compensation of sags of short duration with high magnitudes is also possible.

2.3 Conclusion

The recent advances in Power Electronics, control techniques and availability of microcontrollers for control and fault diagnosis have enabled the realization of advanced utility interfaces economically. With the devices and controllers getting cheaper and the harmonic pollution restrictions getting stricter the advanced utility interfaces will become more popular in future.

Chapter 3

Drives with Capability to Work with Voltage Sag and Under Voltage

3.1 Introduction

As has been discussed in the previous chapter, we need to have an advanced utility interface to make the Adjustable Speed Drive (ASD) capable of working in under voltage condition. Also as discussed, this advanced utility interface has to meet other requirements like unity power factor operation, harmonics free input current, bidirectional power flow. An advanced boost type converter topology commonly called Synchronous link Converter (SLC) has been used as the advanced utility interface. This chapter deals with the details of SLC, its design and working principles, and its implementation as the front end converter for the drive. The simulation studies performed in SABER have been discussed in details.

3.2 Synchronous Link Converter

Uncontrolled rectifiers and line-commutated phase-controlled rectifiers have so far dominated the ac to dc power conversion. Such converters have the inherent drawbacks such as harmonics in input current and output voltage; low input power factor especially at low output voltages. Several applications require ac to dc converters capable of both rectifying and regeneration abilities. Dual converters are used under such circumstances, but with complicated control and power circuits. Synchronous link converter is the best solution under such situations, requiring both rectification and regeneration capabilities. Both single as well as three phase SLC's can be operated at any desired power factor. For having the utility friendly operation, we can make SLC to operate at unity power factor.

3.2.1 Principle of a synchronous link converter

Fig 3.1 shows the circuit of a single-phase synchronous link converter. The switches S_1, S_2, S_3 and S_4 are self-commutating switches such as IGBT's. This circuit resembles that of a voltage source inverter. When the switches are operated with sinusoidal pulse width modulation technique, the converter produces a sinusoidal voltage v_c at the converter input terminals. If the dc link voltage is maintained constant, the magnitude of v_c can be varied by varying the modulation index of the converter. The phase of the converter input voltage v_c, with reference to supply voltage v_s, can be altered by varying the phase of modulating wave and thus switching with respect to v_s.

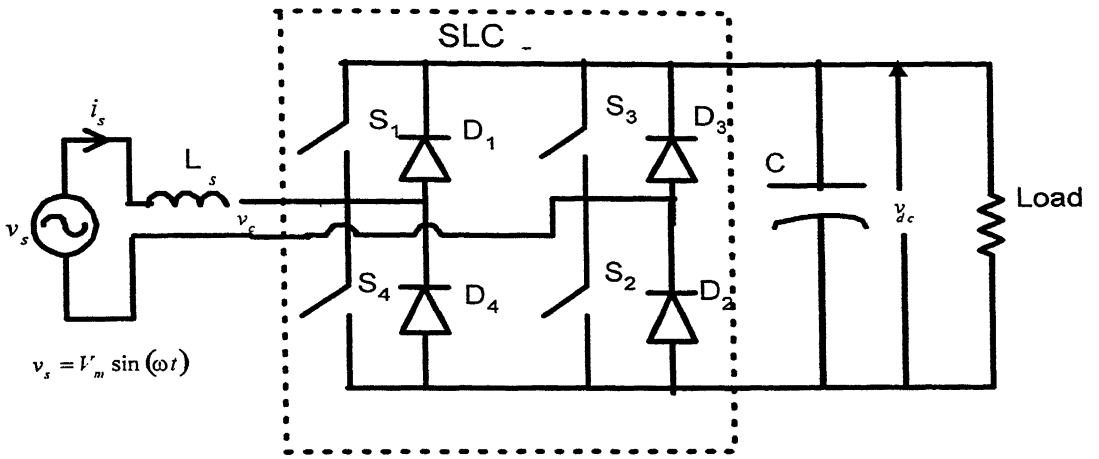
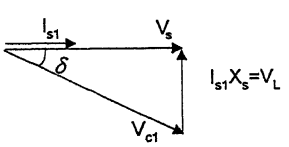
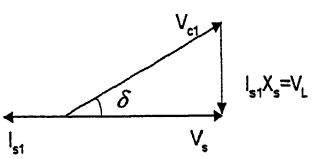


Fig. 3.1 Basic single phase synchronous link converter

Let I_{s1} be the rms phasor of the fundamental component of source current and V_{c1} be the rms phasor of the fundamental component of v_c, under unity power factor (upf) condition. It is assumed that the source voltage, v_s, is sinusoidal without any harmonics. The phasor diagrams for rectification and inversion modes taking $\overline{V}_s$ as the reference are given in Fig. 3.2.



a) Rectification mode



b) Inversion mode

Fig. 3.2 Phasor diagrams of synchronous link converter

$$\vec{V}_s = \vec{V}_{c1} + \vec{V}_L \tag{3.1}$$

$$\vec{V}_L = j\omega L_s \vec{I}_{s1} \tag{3.2}$$

The magnitude and phase of the fundamental converter input voltage V_{c1} are given by,

$$V_{c1} = \sqrt{V_s^2 + V_L^2} \tag{3.3}$$

$$\delta = \tan^{-1}\left(\frac{V_L}{V_s}\right) \tag{3.4}$$

Real power transferred from the source to the converter, $P = V_s I_{s1}$

From the phasor diagram

$$I_{s1} X_s = V_L = V_{c1} sin\delta \tag{3.5}$$

$$V_s = V_{c1} \cos\delta \tag{3.6}$$

$$P = \frac{V_s V_{c1}}{X_L} \sin\delta \tag{3.7}$$

From this we can see that for a given supply voltage V_s and a chosen value of L_s, we can obtain the magnitude and phase of the converter input V_{c1} for upf operation.

The phasor diagrams for u.p.f. operation under forward and reverse power flows are shown in Fig. 3.2, which resembles the vector diagrams of a synchronous machine supplying and regenerating from an active load. The supply inductance (L_s) separates the supply voltage, V_s, and the converter voltage, V_c, and acts as a synchronous link. The converter is, therefore, called a Synchronous Link Converter.

Synchronous link converter works in boost mode. The output dc voltage is fixed and is higher than the peak of the ac supply voltage. Thus ac input voltage is converted into a fixed output dc voltage. The power flow is controlled by controlling the switching pattern. The converter has a sinusoidal input current and a high quality dc output voltage.

These features result in the smaller size of input and output filters and hence result in high efficiency.

In SLC, it is required to regulate the dc link voltage for matching the input power to the converter with the power demand from the dc link. A closed loop dc link voltage control is employed to keep the dc link voltage constant. The converter is operated at u.p.f. for either direction of power flow. For three phase SLC also the principle is same and the calculations are made on per phase basis.

3.2.2 Control techniques for synchronous link converter

For the proper operation of the converter, it has to be operated in a closed loop mode. Various control methods that can be employed with the SLC are as follows.

1. Indirect current control
2. Direct (Hysteresis) current control
3. Predictive current control with fixed switching frequency
4. Load current control

However for the present case, indirect current control at fixed switching frequency is employed for the input current control.

3.2.2.1 Indirect current control

For the proper control of the SLC the dc link, voltage is to be maintained constant by matching the input power with the power demand from the dc link. This power balance is to be maintained at u.p.f. for either direction of power flow.

In the case of indirect current control the ac input current is indirectly controlled by the standard sine PWM, by controlling the fundamental component of converter input voltage v_c.

At any instant of time,

$$v_s = v_c + v_L \tag{3.8}$$

The circuit of Fig 3.3 gives the schematic diagram of indirect current control scheme. The dc link voltage is compared with the reference voltage and the error is processed through a PI controller. This gives the peak value of current. It is then multiplied with reactance (of synchronous link inductor) and phase shifted sine wave and then added to the source voltage to get the modulating signal displaced at δ degrees w.r.t. source voltage. This modulating signal controls the fundamental component of the converter-input voltage and current at unity power factor.

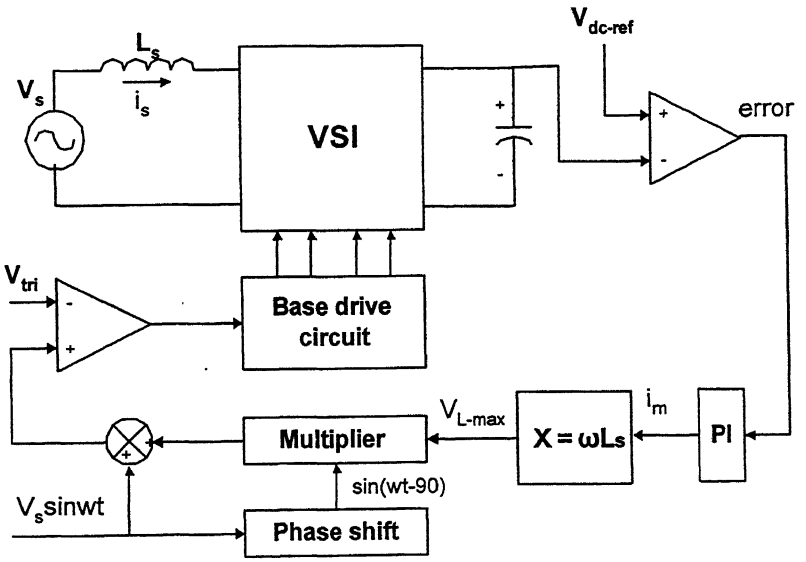


Fig.3.3 Indirect current control scheme for synchronous link converter

The main advantage of this control is that it is a constant switching frequency control therefore the harmonics at the converter input voltage and in converter input current are at the well-defined frequencies. Therefore filters can be designed to suppress those harmonics. However this method of control has the drawbacks of sensitivity to supply parameters and sluggish response.

3.2.3 Design of Synchronous link converter

The selection of various components in a SLC is very crucial for its proper operation. The important aspects of the design are given here.

3.2.3.1 Selection of dc link voltage

The dc link voltage, in general, is decided by the load requirement. Then to ensure proper switching of the devices, the diodes across the devices must be reverse biased under all conditions. So the dc link voltage has to be greater than the peak of the supply voltage, i.e.

$$V_{dc} \geq \sqrt{2} \cdot V_s \tag{3.9}$$

In addition, as per the phasor diagram of Fig. 2.2, the fundamental voltage, V_c at the converter input terminal forms the hypotenuse of the right angled triangle. The magnitude of V_c is also dependent on V_L. Hence the dc link voltage should be sufficiently higher than the peak of the supply voltage to achieve u.p.f. operation for the required load variation.

3.2.3.2 Maximum operating range

The Synchronous Link Converter is controlled to have a constant dc output voltage which is independent of the input supply voltage. Also the output voltage is higher than the peak of supply voltage, so that the anti parallel diodes across the switches are all reverse biased. Hence for the proper operation of synchronous link converter, there is a restriction on the output voltage. For unity power factor operation we have

$$V_{c1} = \sqrt{V_s^2 + (I_{s1}X_s)^2} \tag{3.10}$$

$$V_{c1} = \frac{M_f V_{dc}}{\sqrt{2}} \tag{3.11}$$

for pulse width modulation with unipolar switching. Substituting equation (3.11) in equation (3.10) and solving for I_{s1} for M_f=1 we get

$$I_{s1b} = \sqrt{\frac{0.5V_{dc}^2 - V_s^2}{X_s}} \tag{3.12}$$

Where I_{s1b} is the maximum permissible rms input current (also known as current distortion limit) for given value of dc link voltage V_{dc}, supply voltage V_s and synchronous link inductor L_s. It is evident that the operating region of a Synchronous Link Converter is higher with lower value of Synchronous link inductor and higher value of dc link voltage.

3.2.3.3 Selection of synchronous link inductor

For the deciding the value of Synchronous Link inductor, the following considerations have to be made.

For lower harmonic component in the source current drawn by Synchronous Link Converter, it is essential that the maximum modulation index at which the converter operates is close to unity, as permitted by the turn off time of devices used. Under such conditions, the magnitude of converter input voltage V_{c1} varies over wide range, with the change in power demand on the converter. This will ensure that the control will be less sensitive to errors. Assuming that the converter operates with unity power factor, we can obtain expression for the modulation index as given by the following equation

$$M_f = \frac{\sqrt{V_s^2 + (I_{s1}X_s)^2}}{\frac{V_{dc}}{\sqrt{2}}} \tag{3.13}$$

The equation (3.13) suggests that if a very low value of inductor is used, the range of variation of modulation index (M_f) and hence converter input voltage V_{c1} becomes very much limited (with the change in load on the converter) and hence control becomes sensitive to errors. For maximum allowable modulation index, the maximum limiting value of the inductor can be obtained as follows:

From the Fig 3.2 we have

$$V_s = V_{c1}\cos\delta \tag{3.14}$$

$$I_{s1} = \frac{\sqrt{V_s^2 - V_{c1}^2}}{X_L} \tag{3.15}$$

$$P_{in} = \frac{V_s V_{c1}\sin\delta}{X_L} \tag{3.16}$$

$$P_{out} = V_{dc} I_d \tag{3.17}$$

For loss less converter we have, $P_{in} = P_{out}$

$$\frac{V_s V_{c1} \sin\delta}{X_L} = V_{dc} I_d \tag{3.18}$$

From equation (3.18) solving for L_s we get,

$$L_s = \frac{V_{c1} V_s \sin\delta}{\omega V_{dc} I_d} \tag{3.19}$$

For a given dc link voltage the maximum input voltage is given by

$$V_{c1\max} = \frac{M_{f\max} V_{dc}}{\sqrt{2}} \tag{3.20}$$

Where, $M_{f\ max}$ = the maximum modulation index as decided by turn off time of the devices used. Now

$$\delta_{\max} = \cos^{-1}\left(\frac{V_s}{V_{c1\max}}\right) \tag{3.21}$$

Substituting the equation (3.21) in equation (3.19) we get

$$L_{s\max} = \frac{V_s V_{c1} \sin\delta_{\max}}{\omega V_{dc} I_{d\max}} \tag{3.22}$$

Where $I_{d\ max}$ = maximum value of the dc link current.

The dominant harmonics in the input voltage of the Pulse Width Modulated converter will occur around the frequency $2f_{sw}$ where f_{sw} is the switching frequency. The inductor should be designed to keep the ripple in the input current at this frequency around certain percent of the maximum input current.

The conservative value of the synchronous link inductor to keep the ripple in input current within this limit can be obtained as follows.

For a single phase unipolar pulse width modulated converter the dominant harmonic component present in the voltage is around the frequency $2f_{sw}$ and typically has a magnitude of 39.25% of the fundamental component of the voltage on ac side of the Voltage Source Inverter [[ref; Ned Mohan]].

$$V_{ch} = 0.3925 * \frac{M_f V_{dc}}{\sqrt{2}} \tag{3.23}$$

The value of synchronous link reactance at effective switching frequency is

$$X_L = 2\pi f_{sw} L_s \tag{3.24}$$

where L_s is the synchronous link inductance. Thus the most dominant harmonic component of current will be

$$I_{sh} = \frac{V_{ch}}{2\pi f_{sw} L_s} \tag{3.25}$$

Assuming I_{sh} is limited to x% of I_{s1} we get

$$L_s = \frac{100 V_{ch}}{2\pi f_{sw} I_{s1} x} \tag{3.26}$$

where $L_s \leq L_{smax}$.

As the converter operates at u.p.f., if the converter losses are neglected, the value of source current can be taken as

$$I_{s1} = \frac{V_{dc} I_d}{V_s} \tag{3.27}$$

Accounting for harmonics and converter losses, the inductor rating can be selected to be 10% higher than I_{s1max}.

3.2.3.4 Selection of dc link capacitor

The important factor that decides the selection of dc link capacitor is the allowable ripple in the dc link voltage. Normal limit is 5% of the rated dc link voltage. So the value of capacitance, C, is given by

$$C \geq \frac{100 V_s I_{s1}}{2\omega V_{dc}^2 x} \tag{3.28}$$

Where, x is the % of ripple in the dc voltage.

The rms current through the capacitor is given by

$$I_{crms} = \frac{I_d}{\sqrt{2}} = \frac{V_s I_{s1}}{\sqrt{2} V_{dc}} \tag{3.29}$$

But for this Voltage Sag ride through application the capacitance value has to be decided based on a few more aspects. We know here that the voltage across the dc link capacitor remains constant, in steady state, because the power supplied by the front end converter is equal to the power taken by the inverter on the other side of the capacitor. There is ripple in V_{dc} due to second harmonic component of current and the capacitor supplies the reactive power only. Whenever any voltage sag, or swell or load variation occurs the power balance is lost, and the difference in the two powers is taken from or supplied to the capacitor. Thus the capacitor voltage starts falling or rising. Then the closed loop controller again builds up the balance between the powers of the two converters and brings the capacitor voltage back to reference value. As the controller takes some time to regain the balance the capacitance value should be large enough to supply power for this much time.

The dc voltage rating of the capacitor depends on the dc link voltage and is calculated by taking a safety factor of 1.25 times of that of rated dc link voltage, to account for over charging during the transients.

3.3 Synchronous Link Converter as the Front-end Converter of the Drive

Single as well as three phases SLC's have been used as the front-end converter for the Voltage Source Inverter Induction Motor Drive. The operating principle, control strategy and the design criteria of the SLC, for this application, have already been discussed. The proposed topologies of single and three phases are shown in Fig. 3.4 and Fig. 3.5 below.

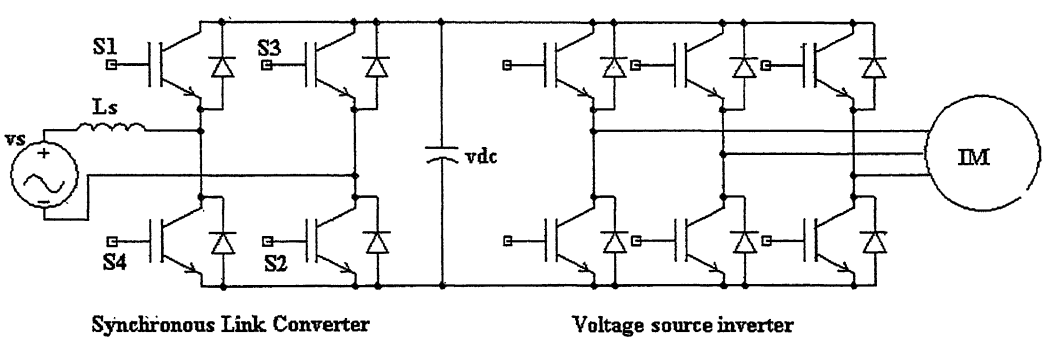


Fig. 3.4 Single phase SLC as the front end converter of the drive

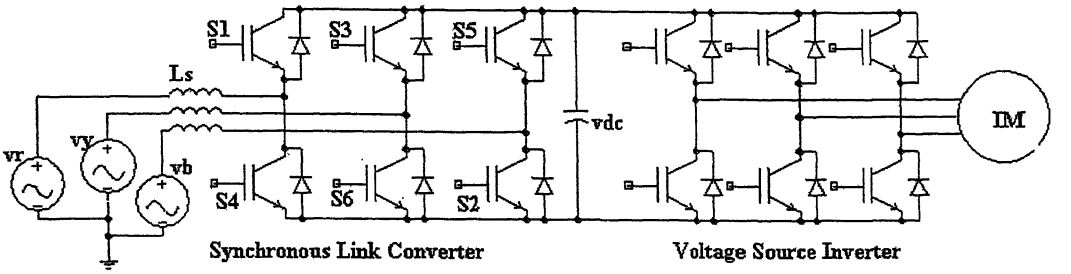


Fig. 3.5 Three phase SLC as the front end converter of the drive

Since the front-end converter, for operation of the Drive, only has to process the active power delivered to the load, the SLC is operated at unity displacement power factor. For a typical motor load operating at a lagging power factor, the front-end converter processes less current than the load side inverter. Considering three phase SLC topology shown in Fig.3.5, for equivalent load side inverter and front-end converter ratings, it follows that some percentage of the current capacity of the SLC can be used to provide voltage sag ride-through to the Drive. In the following derivation and discussion, it is assumed that all quantities are rms, unless otherwise quantified.

The dc-bus voltage drops during a sag condition due to an active power imbalance between the front and load end converters which results in energy being extracted from the dc-link capacitor. To regulate the dc-bus voltage of the Drive during sags, it is,

therefore, necessary to ensure that the same active power is supplied by the SLC during the sag as before the sag, i.e.,

$$\sqrt{3}V_{ll}I_{l} = \sqrt{3}V_{ll}(1-sag)I_{l,sag} \tag{3.30}$$

where, V_{ll} is the line to line supply voltage, I_l is the line or phase current. Under sag conditions, the input line voltage is equal to $V_{ll}(1- sag)$, where sag expresses the sag magnitude in per unit. This means that the input supply current will have to increase by the factor k where

$$k = \frac{I_{l,sag}}{I_{l}} = \frac{1}{1-sag} \tag{3.31}$$

The maximum sag the drive can withstand is, therefore, dependent on the SLC's devices' current ratings and the load condition of the Drive. In order to quantify the maximum sag that ride-through can be provided for by drawing more current through the front end converter, it is assumed that the load side inverter and the front-end converter have similar ratings. The inverter devices are rated at the maximum dc-bus voltage and the current rating is determined by the worst case condition of supplying rated apparent power, $S_{inv,rated}$ to the load at the minimum fundamental output voltage, $V_{o,min}$ i.e.,

$$I_{inv,rated} = \sqrt{2}\frac{S_{inv,rated}}{\sqrt{3}V_{o,\min}} \tag{3.32}$$

Assuming the same device rating for the SLC, the peak input current needs to be limited to less than $I_{inv,rated}$. Since the SLC is controlled to operate at unity power factor, it only supplies the active power to the load. Based on this discussion, the resulting rms input supply current during the sag is limited to

$$I_{l,sag} = \frac{S_{inv} DPF}{V_{ll}(1-sag)\eta_{inv}\eta_{SLC}} \leq \frac{S_{inv,rated}}{\sqrt{3}V_{o,\min}} \tag{3.33}$$

Consequently, for similar front and load end converter ratings, the sags that can be compensated for are limited to

$$sag_0 \leq 1 - \frac{DPF \times S_{inv} V_{o,\min}}{S_{inv,rated} V_{ll} \eta_{inv} \eta_{SLC}} \tag{3.34}$$

For example, for an induction motor load operating at 90% load and a displacement power factor of 0.9, with rectifier and inverter efficiencies of 95% and, voltage sag ride-through for sags of up to 19% and of any duration can be provided without de-rating of the SLC. By de-rating the front-end converter, ride-through for sags of higher magnitudes can be provided. The sag magnitude, sag_d, for which ride-through can be provided by de-rating the front-end converter depends on the factor, k_d, by which the rating of the this converter is increased and on the sag ride-through capability sag_0 of the drive before de-rating, i.e.,

$$sag_d = 1 - \frac{1-sag_0}{k_d} \tag{3.35}$$

This design concept can also be used in retrofit applications by connecting the active front end converter with voltage sag ride-through control in parallel with the existing diode bridge rectifier of the drive. The active rectifier can also be used in a system with several inverters connected to a common dc bus. Similarly, in case of single phase SLC topology also we can calculate the ratings and Voltage Sag ride-through capability of the Drive.

3.4 Simulations

To verify the feasibility of the proposed ride-through system, simulation studies have been performed for both the topologies. The elaborate circuits have been simulated in a standard circuit simulation software, SABER simulator, which can simulate the system very near to the manner it is practically implemented. The control circuits can also be simulated with analog and digital components.

3.4.1 Single Phase SLC

The Single phase SLC used as the front-end converter for the Drive has been designed and the parameters have been calculated based on the principles and criteria already explained. For ease of organization the complete circuit has been split into five sheets. There are two sheets for Power circuit, one (Fig. 3.6) having input supply and SLC and the other (Fig. 3.7) having the dc link capacitor, load side inverter, the induction motor and its load. Power circuit consists of converters with switches, diodes and power supplies. Sensors are provided to sense the input voltage and dc link voltage. There is one sheet (Fig. 3.8) for closed loop control circuit of the SLC. It consists of control parts like PI controller, sub tractor, adder, multiplier, reference generator, limiter etc. And there are two sheets for the Gate drive circuits, one (Fig. 3.10) for driving the switches of the SLC and the other (Fig. 3.9) for the switches of the load side inverter. The gate drive circuits generate the gate pulses by comparing the reference signals with the fixed frequency triangular wave. In SABER, same page connectors are used to connect signals from one page to another page.

The voltage sources and semiconductor switches used in the simulations are ideal. The simulations have been done for voltage variation from rated voltage to 40% sag and vice versa. Fig. 3.13 and Fig. 3.14 show the dc link voltage and current profile for a step change of the supply voltage. Fig. 3.15 and Fig. 3.16 show voltage variation from rated to 20% swell and vice versa. The worst case conditions of having supply voltage variation from 20% swell to 40% sag and vice versa have also been shown in Fig. 3.17 and Fig. 3.18. Power flow reversal from rectification to inversion and back has been shown in Fig. 3.19 and Fig. 3.20. From all these observations we find that with this topology of having SLC as the front end converter and indirect current control scheme the dc link voltage is maintained very close to the reference value. And the current drawn from the supply is almost sinusoidal (low in harmonics) and in phase with the voltage. The steady state condition of voltage and current for forward power flow has also been shown in Fig .3.11. The current harmonics have been given in Fig. 3.12 which shows the current is very close to sinusoidal.

The parameters used in the simulations are given below

Supply voltage	: 220 V, 50 Hz, a.c. Single Phase
Synchronous Link Inductor	: 22.9 mH
DC Link Capacitance	: 3300 μF
DC Link Voltage	: 380 V
Switching Frequency of SLC	: 5 kHz
Switching Frequency of inverter	: 5 kHz

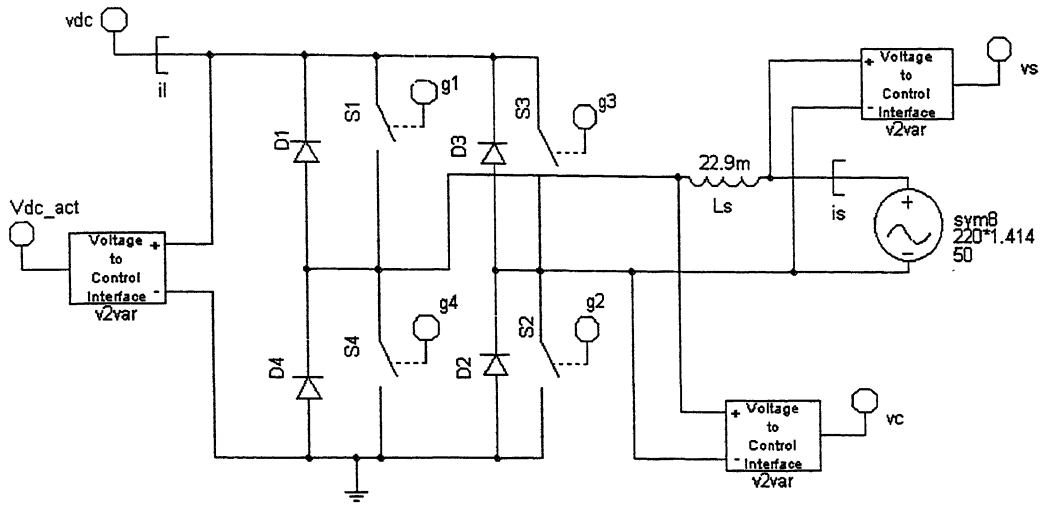


Fig. 3.6 Power circuit showing SLC

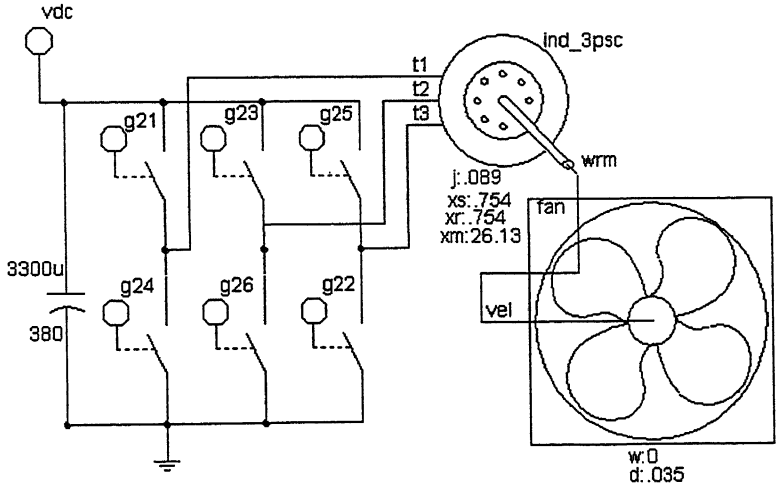


Fig. 3.7 Power circuit load side inverter and motor load

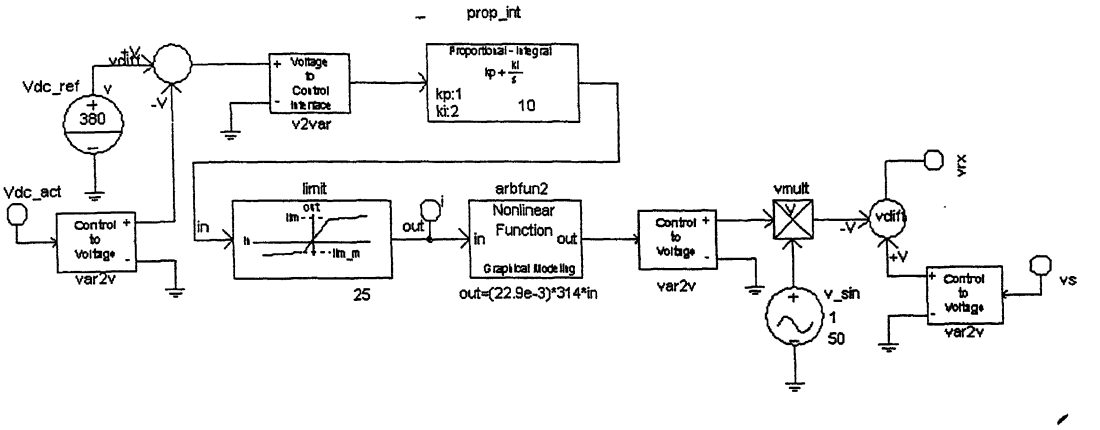


Fig. 3.8 Closed loop control circuit

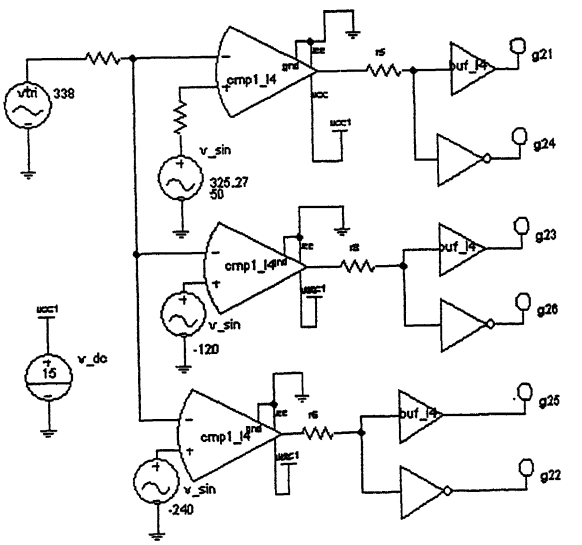


Fig. 3.9 Gate drive circuit for load side inverter

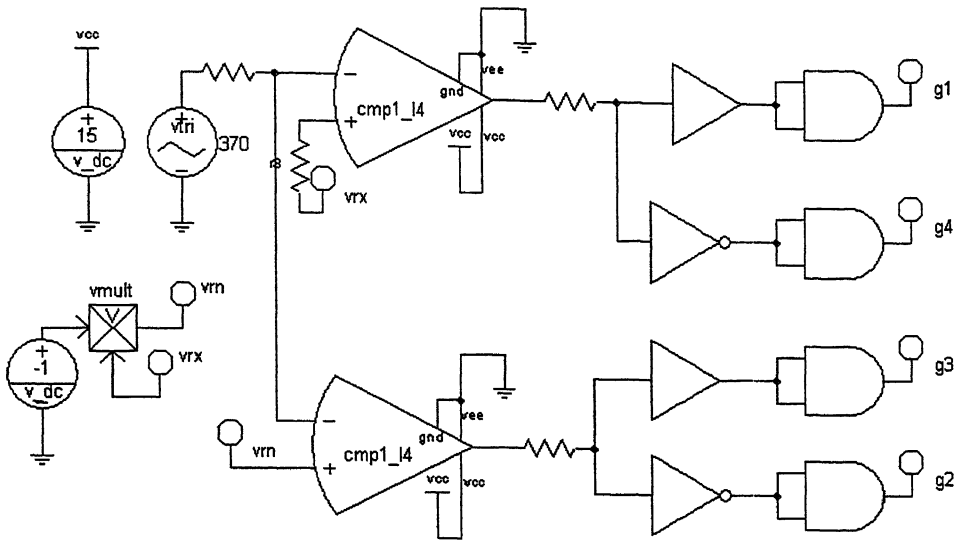


Fig. 3.10 Gate drive circuit for SLC

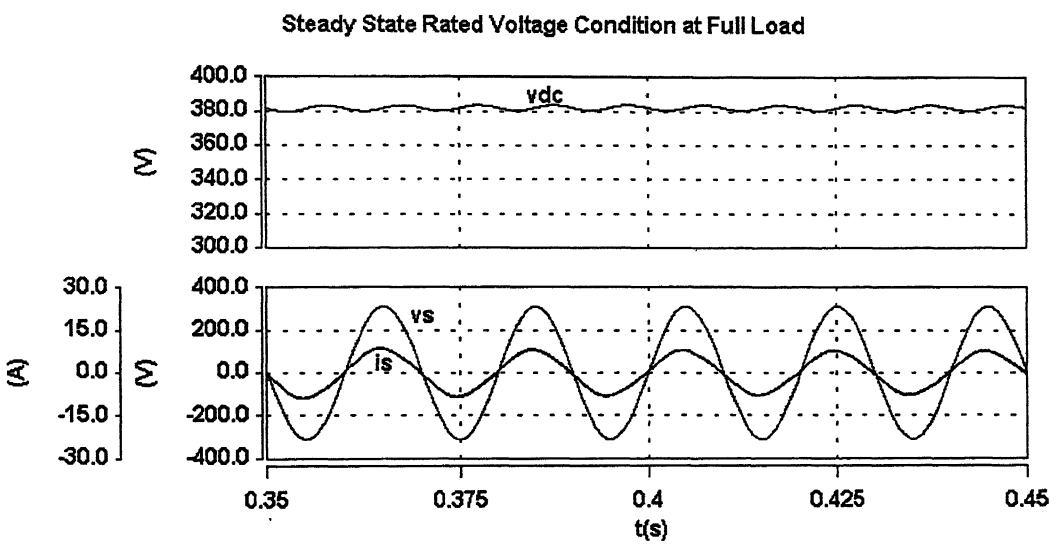


Fig. 3.11 Steady state rated voltage condition

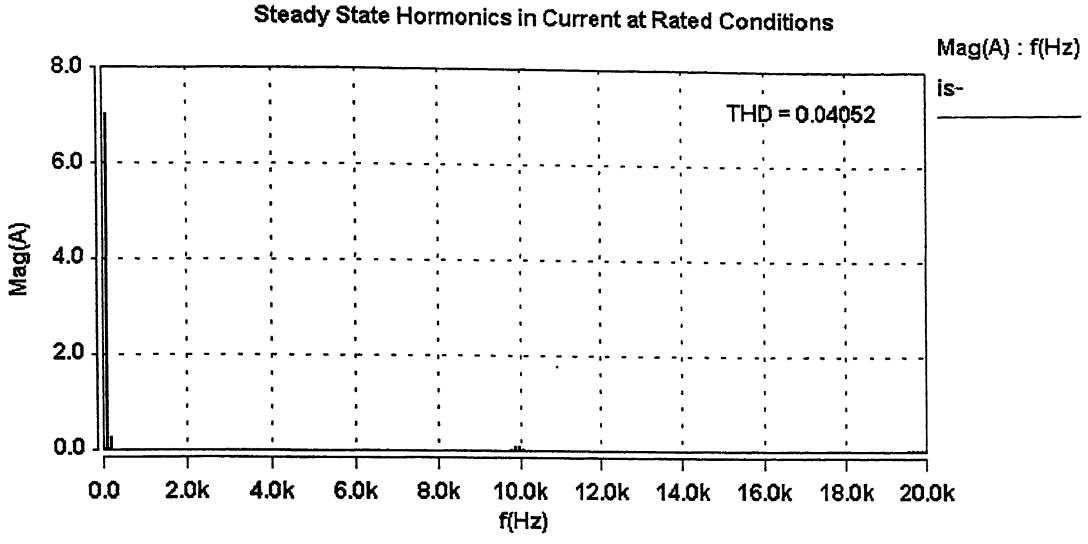


Fig. 3.12 Steady state current harmonics at rated conditions

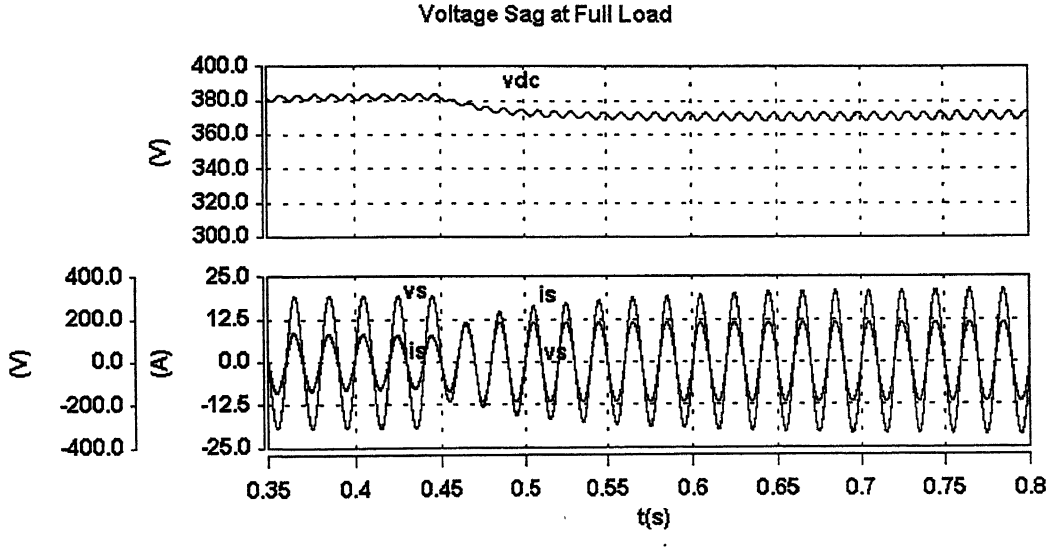


Fig. 3.13 Voltage variation from rated to sag condition at full load

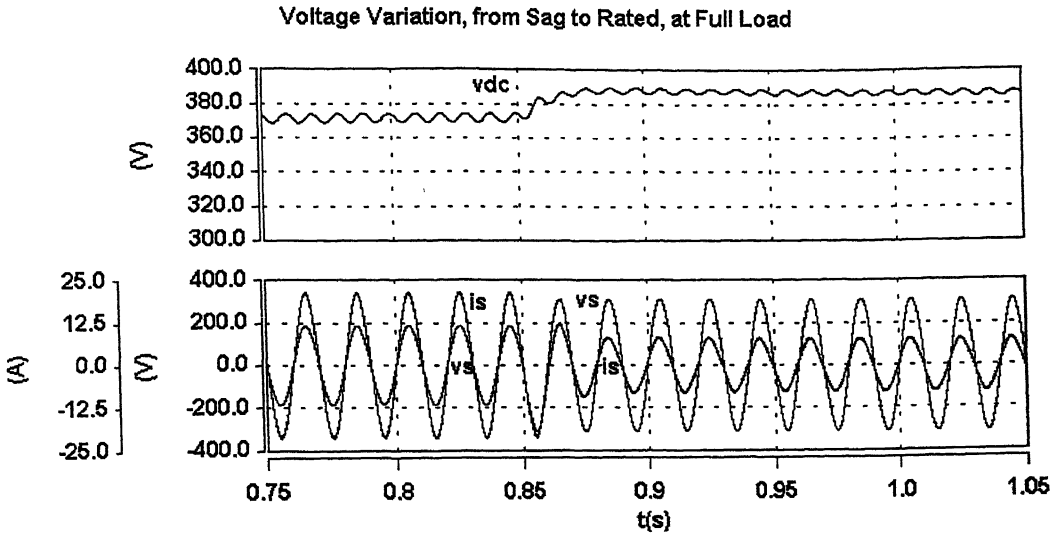


Fig. 3.14 Voltage variation from sag to rated condition

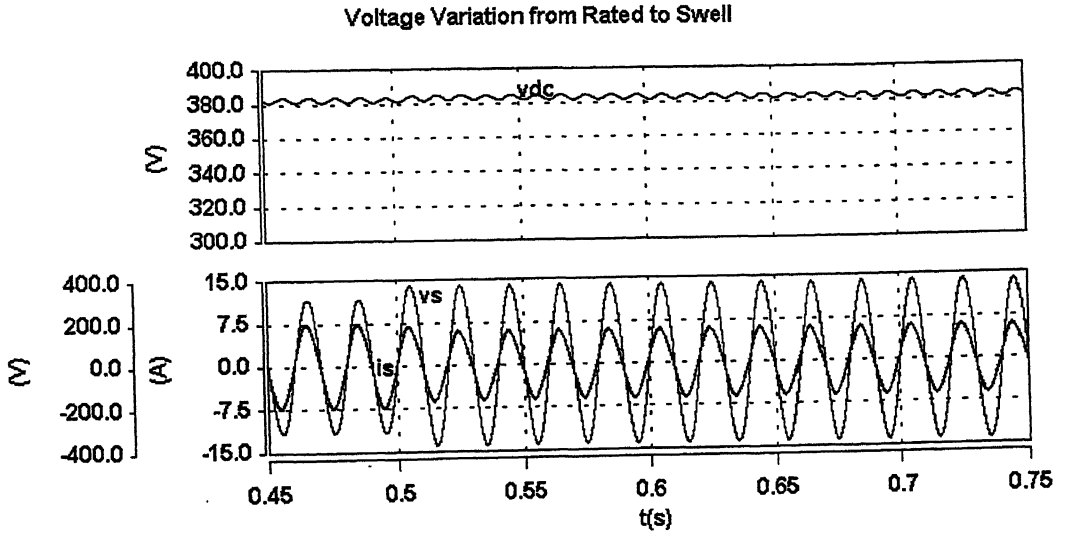


Fig. 3.15 Voltage variation from rated to swell condition

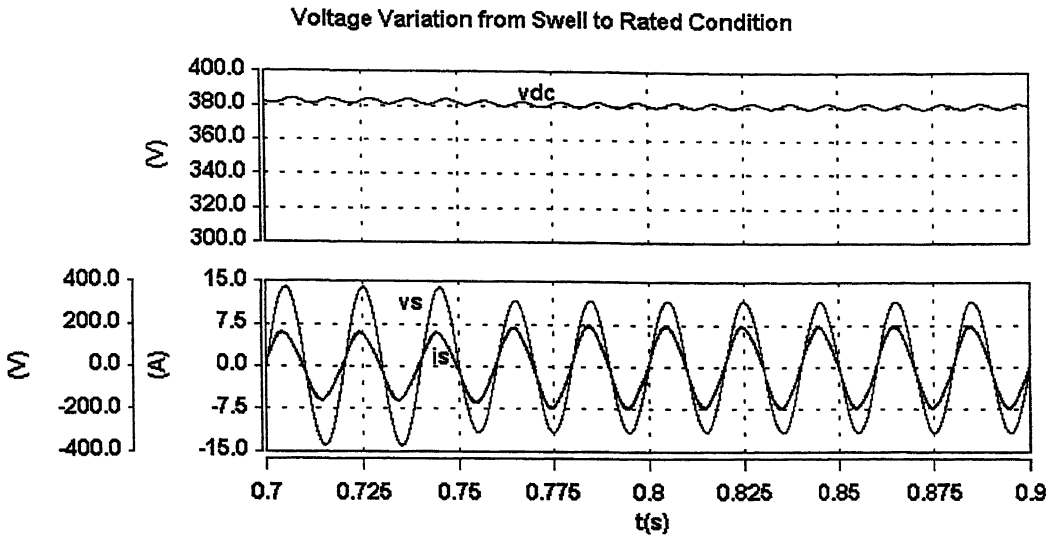


Fig. 3.16 Voltage variation from swell to rated condition

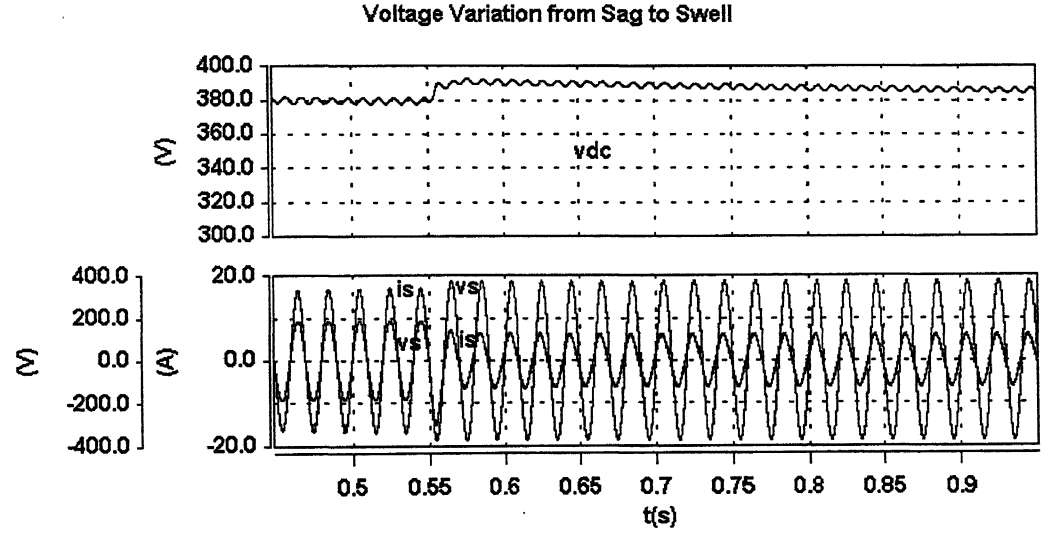


Fig. 3.17 Voltage variation from sag to swell condition

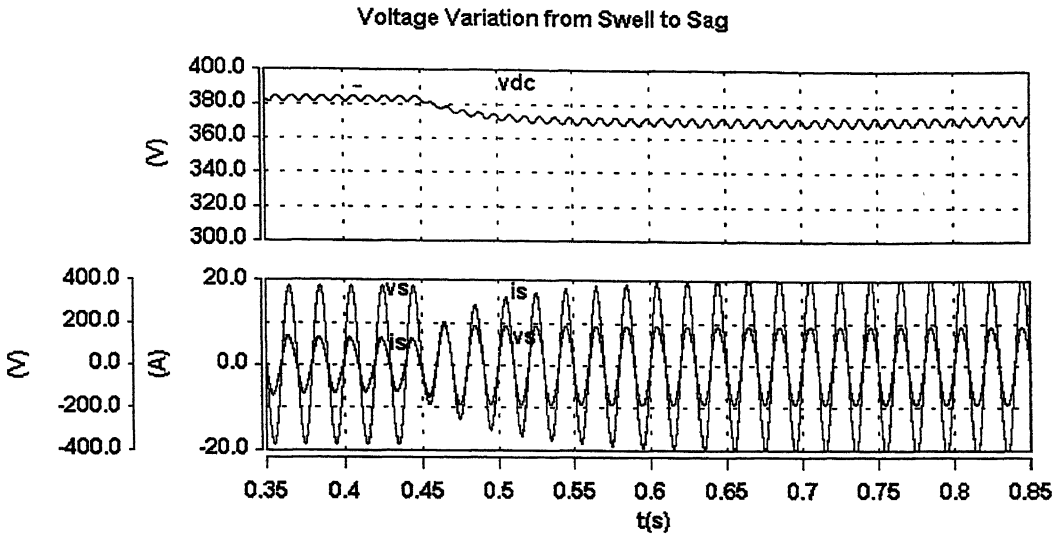


Fig. 3.18 Voltage variation from swell to sag condition

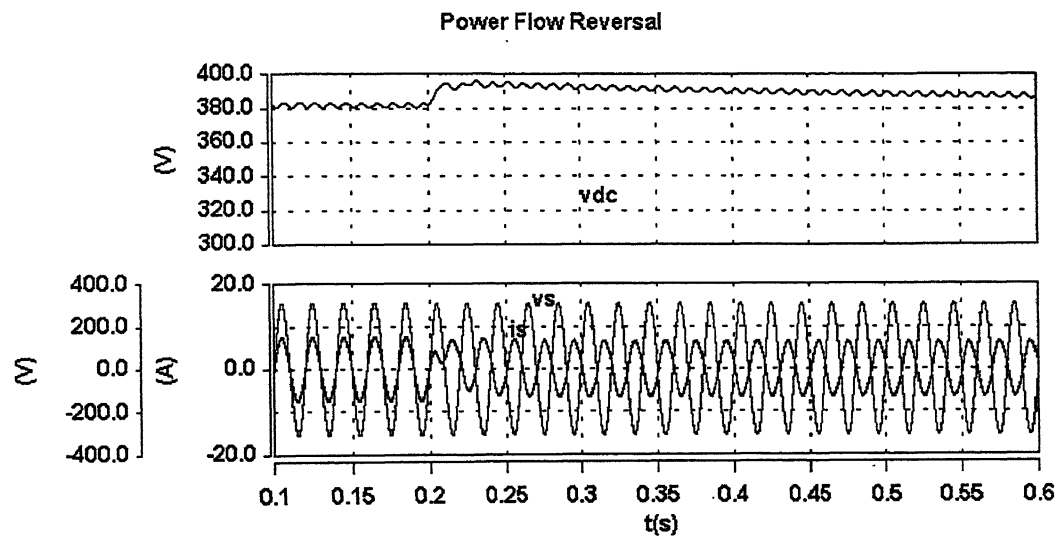


Fig. 3.19 Power flow reversal, rectification to inversion

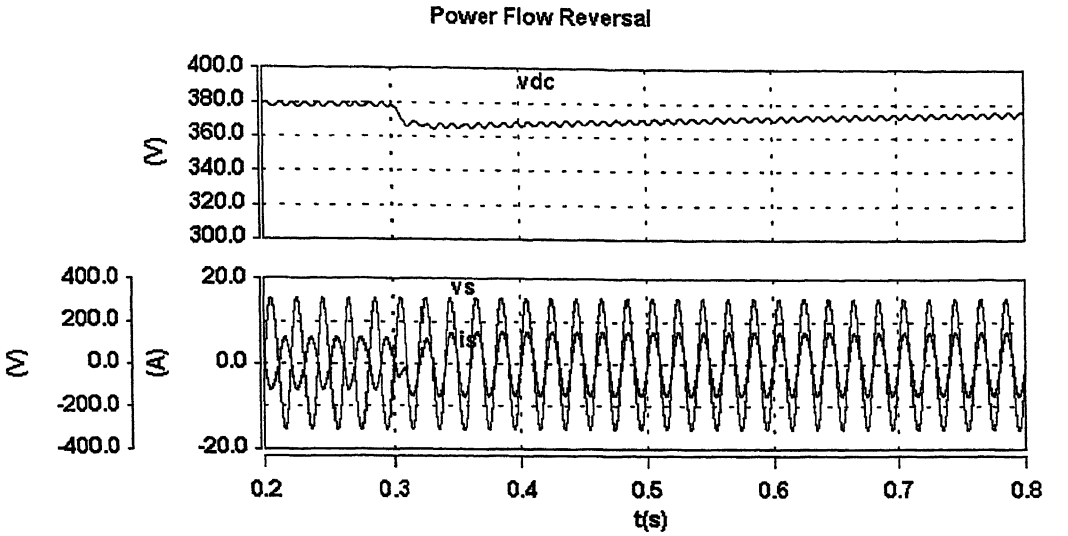


Fig. 3.20 Power flow reversal, inversion to rectification

3.4.2 Three Phase SLC

The three phase SLC topology has also been used as the front-end converter for the Drive to act as the advanced utility interface with the three phase supply. It has also been designed and the parameters have been calculated based on similar principles and criteria already discussed. For simulation studies in case of three phase the assumption has been made that sag occurs in all the three phases simultaneously and by same magnitude. The organization of the simulation circuits in this case is very similar to the single phase one.

The voltage sources and semiconductor switches used in the simulations are ideal. These simulations have also been done for voltage variation from rated voltage to 40% sag and shown in Fig. 3.28. It show the dc link voltage and current profile for a step change of the supply voltage. Fig. 3.31 shows voltage variation from rated to 20% swell. The worst case conditions of having supply voltage variation from 20% swell to 40% sag and vice versa have also been shown in Fig. 3.33 and Fig. 3.34. Power flow reversal from rectification to inversion and back has been shown in Fig. 3.35 and Fig. 3.36. From all these observations we find that with this topology of having SLC as the front end converter and indirect current control scheme the dc link voltage is maintained very close to the reference value. And the current drawn from the supply is almost sinusoidal (low in harmonics) and in phase with the voltage. The steady state conditions of voltage and current for forward and reverse power flow at rated as well as sag condition have also been shown in Fig. 3.26, Fig. 3.29 and Fig. 3.37. The current harmonics have been given

in Fig. 3.27, Fig. 3.30 and Fig. 3.32 which show the current harmonics are within acceptable limits.

The parameters used in the simulations are given below

Supply voltage	: 400 V, 50 Hz, a.c. 3-ϕ
Synchronous Link Inductor	: 20 mH
DC Link Capacitance	: 3300 μF
DC Link Voltage	: 750 V
Switching Frequency of SLC	: 5 kHz
Switching Frequency of inverter	: 5 kHz

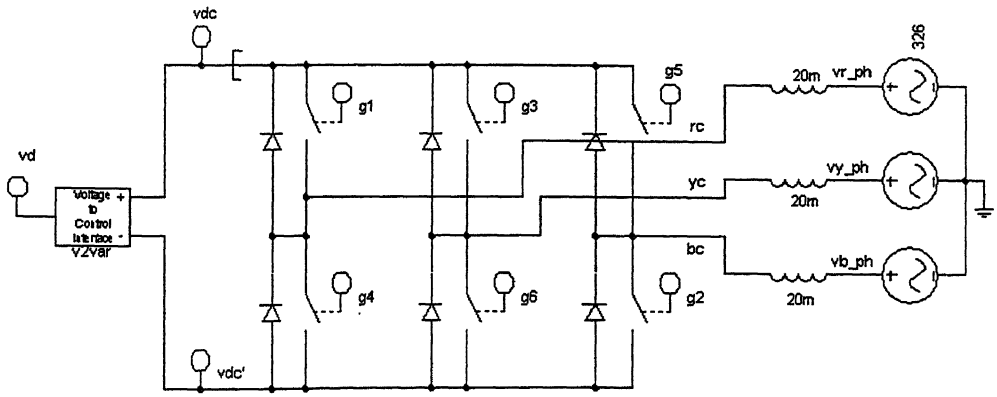


Fig. 3.21 Power circuit showing three phase SLC

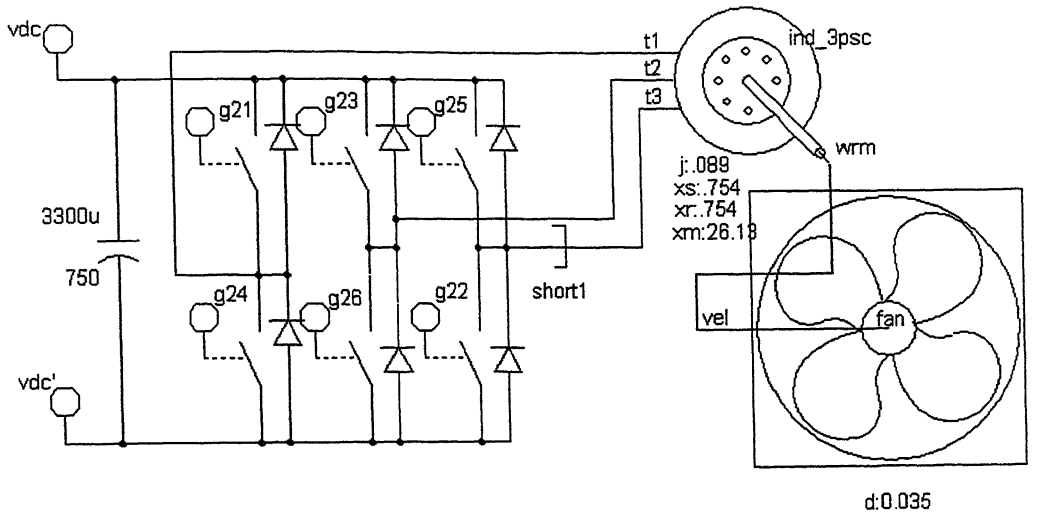


Fig. 3.22 Power circuit showing load and load side inverter with the dc link

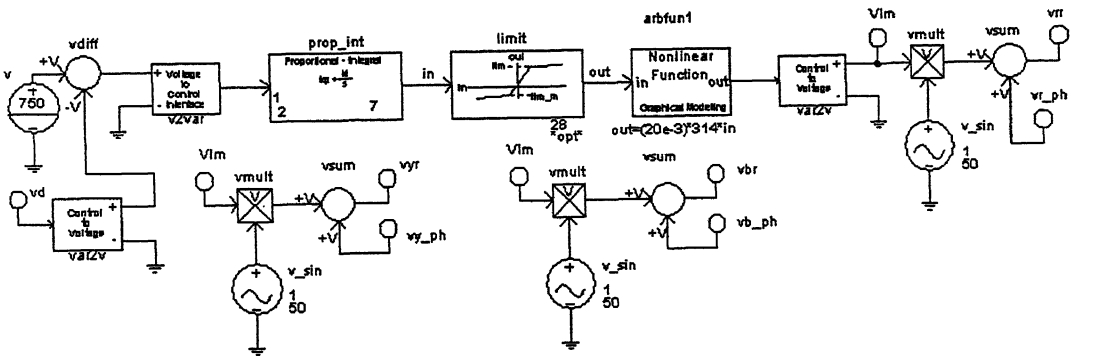


Fig. 3.23 Closed loop control circuit for the three phase SLC topology

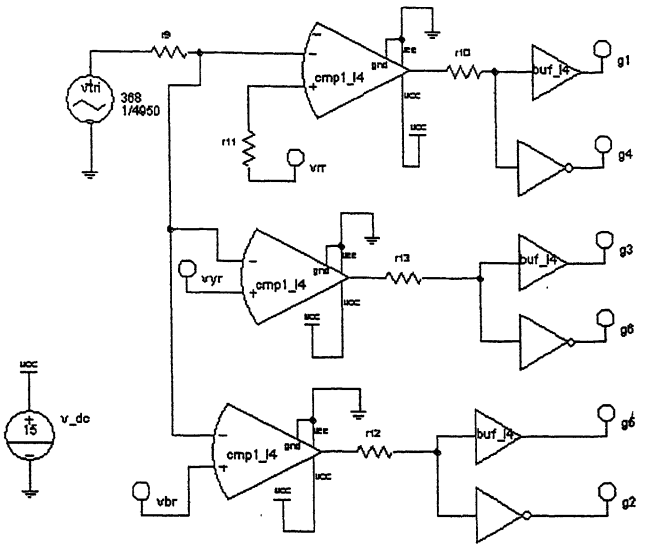


Fig. 3.24 Gate drive circuit for the SLC

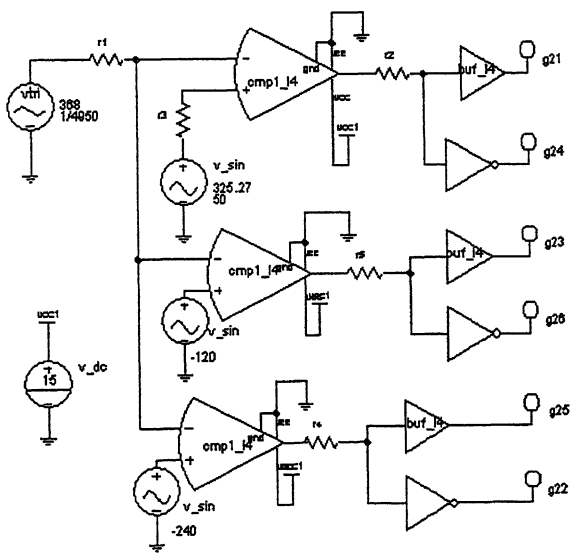


Fig. 3.25 Gate drive circuit for the load side inverter

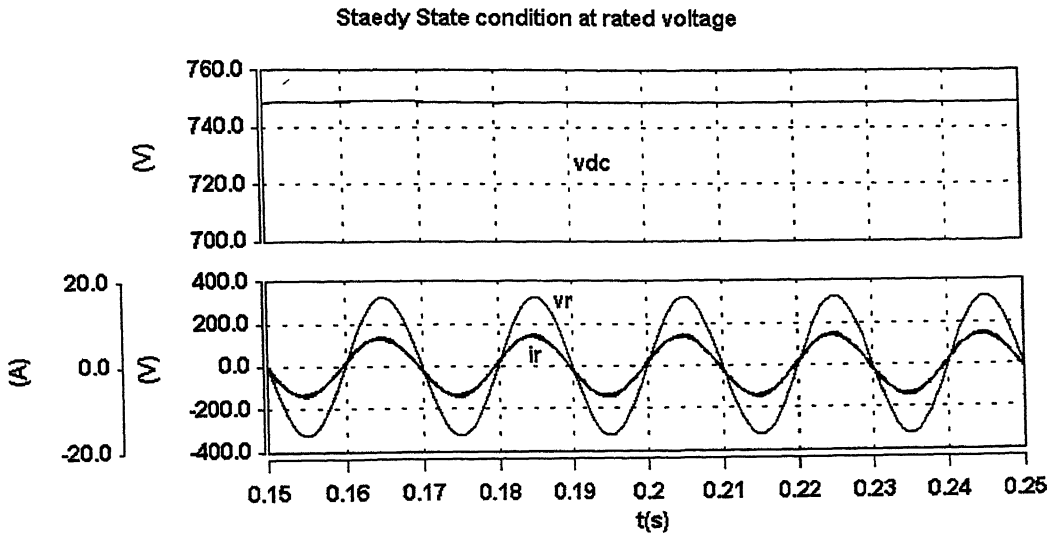


Fig. 3.26 Steady state rated voltage condition

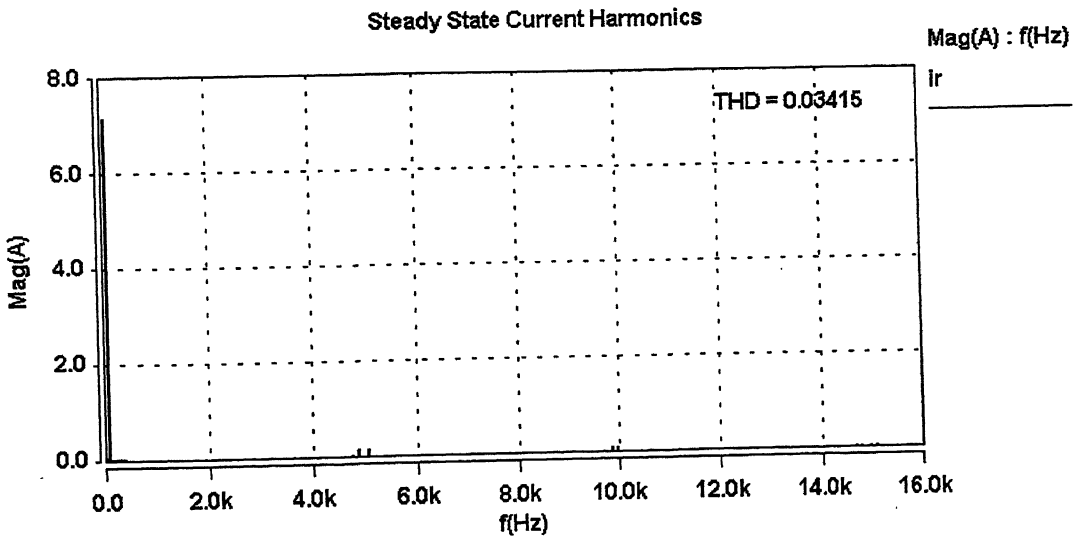


Fig. 3.27 Steady state current harmonics under rated conditions

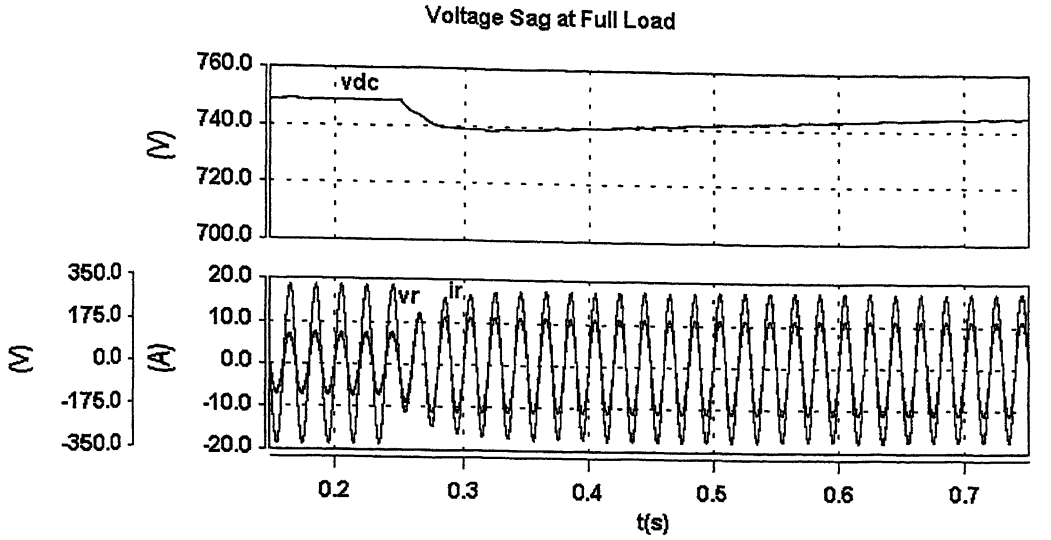


Fig. 3.28 Voltage variation from rated to sag condition

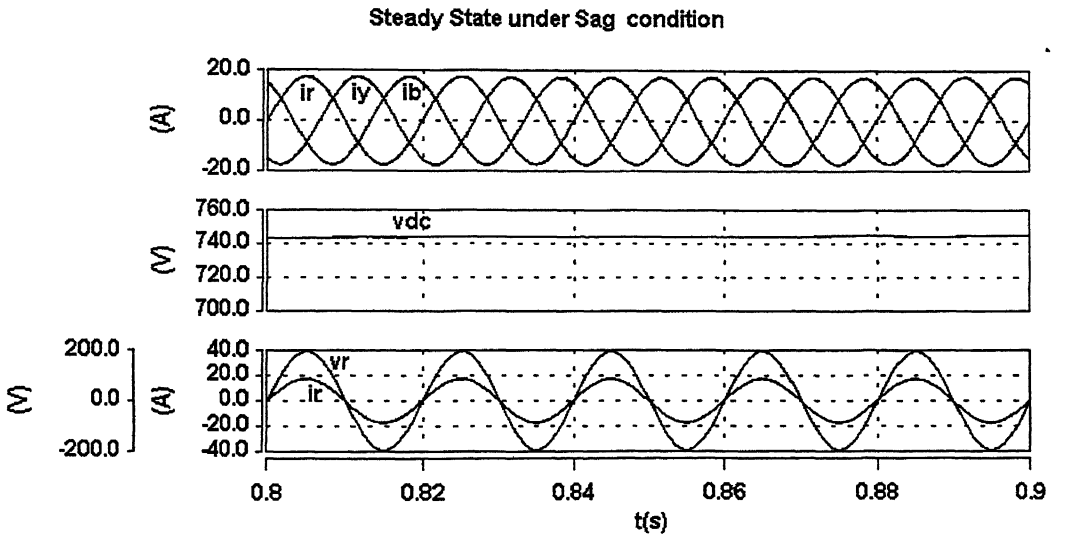


Fig. 3.29 Steady state condition under voltage sag

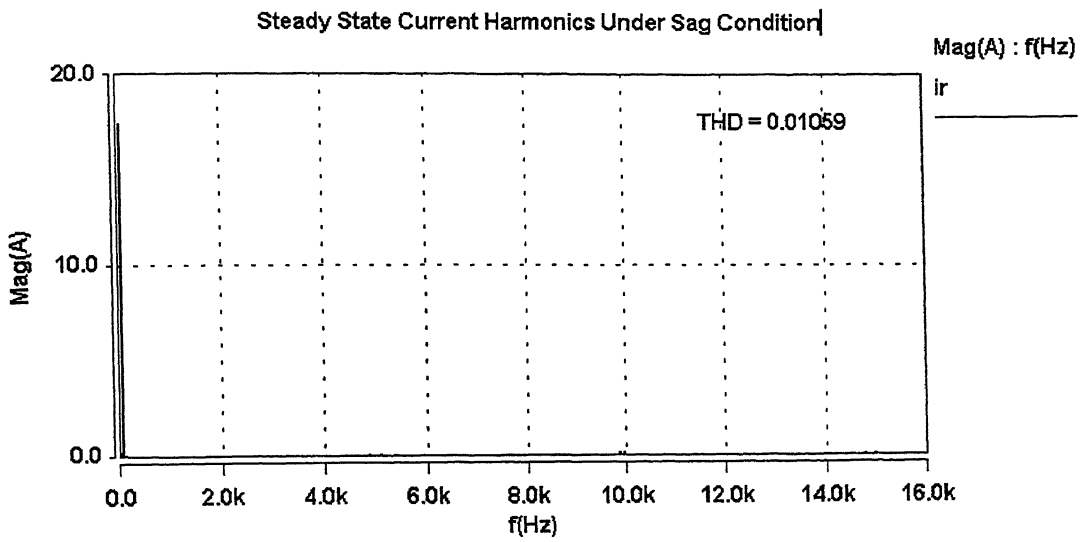


Fig. 3.30 Steady state current harmonics under voltage sag condition

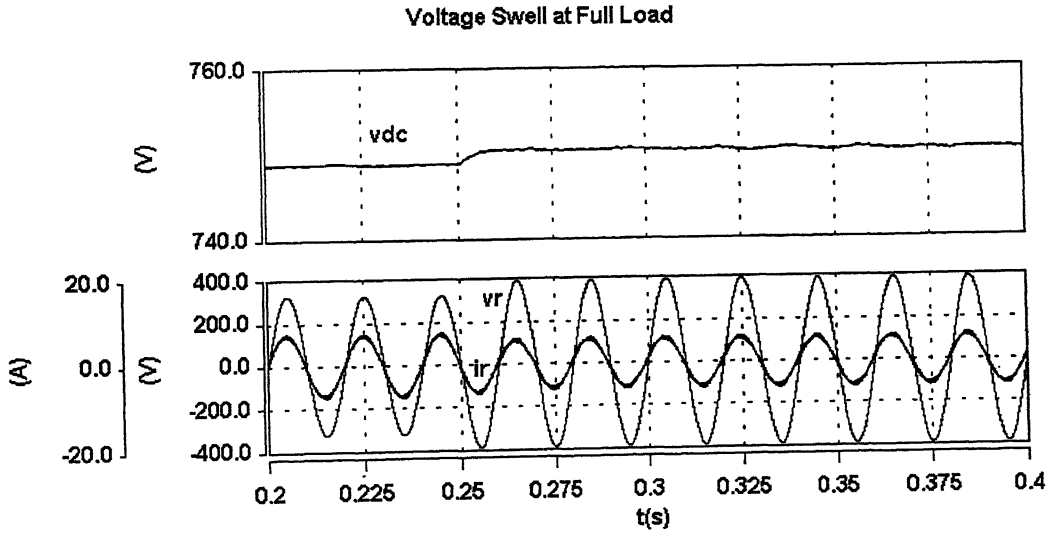


Fig. 3.31 Voltage variation from rated to swell condition

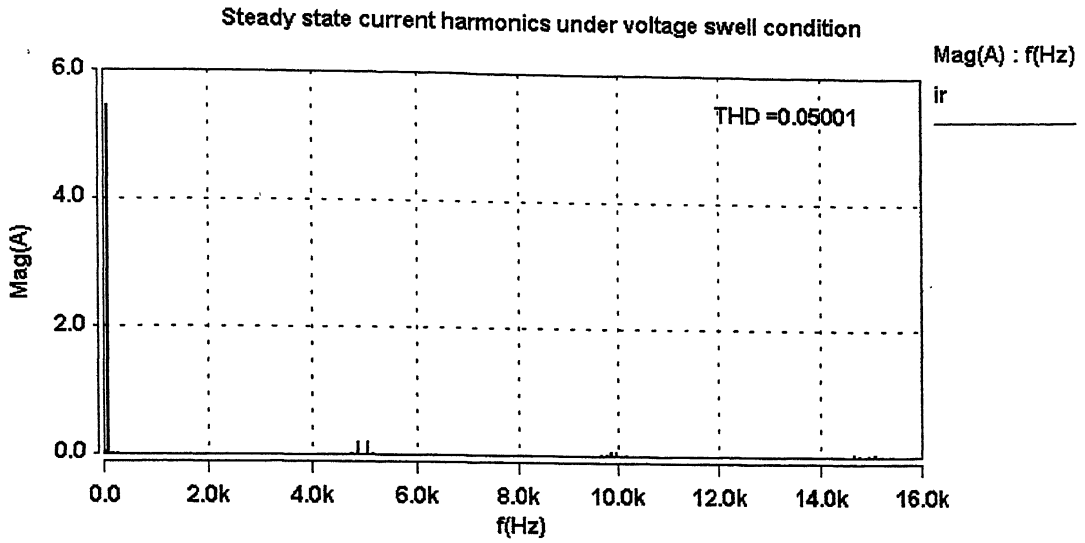


Fig. 3.32 Steady state current harmonics under voltage swell condition

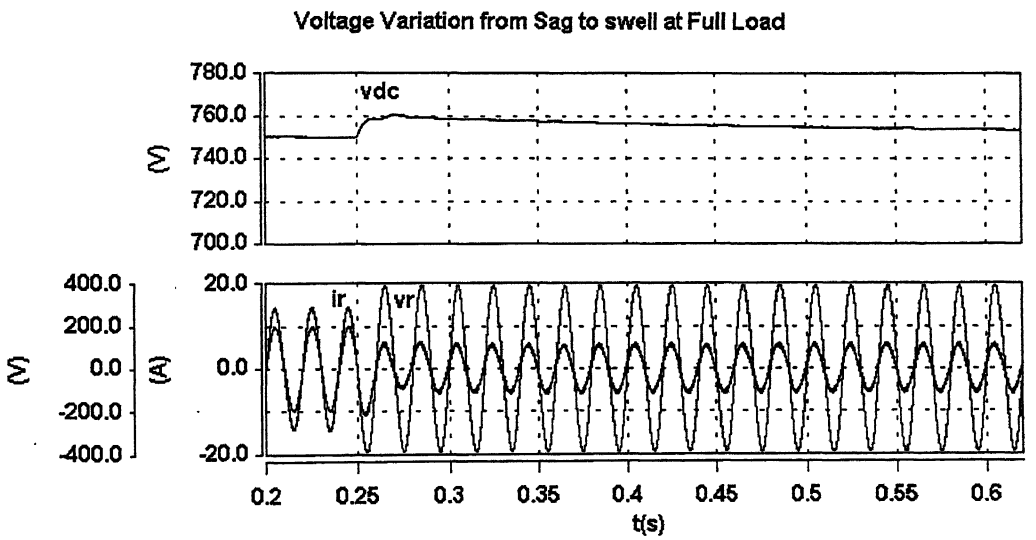


Fig. 3.33 Voltage variation from sag to swell condition

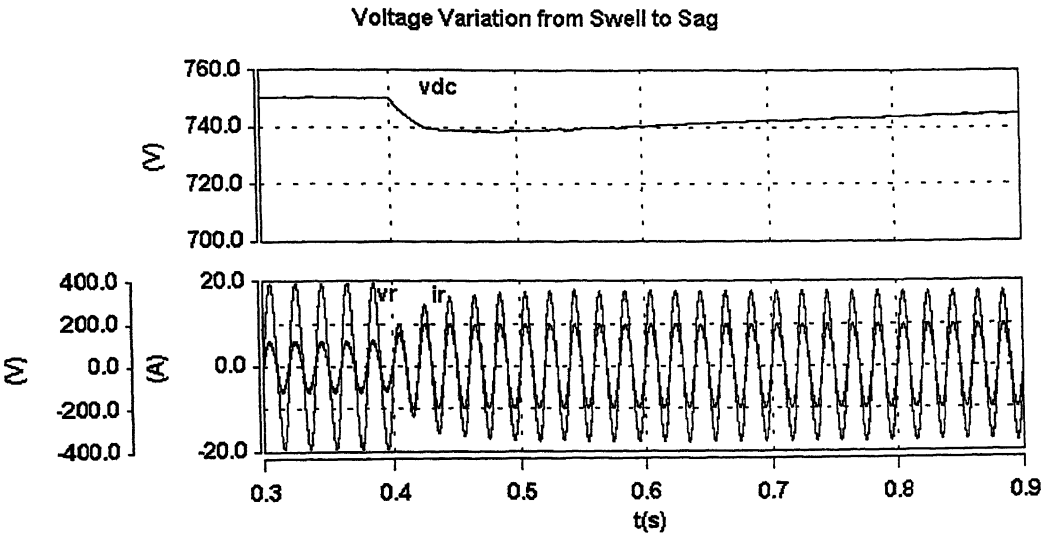


Fig. 3.34 Voltage variation from swell to sag condition

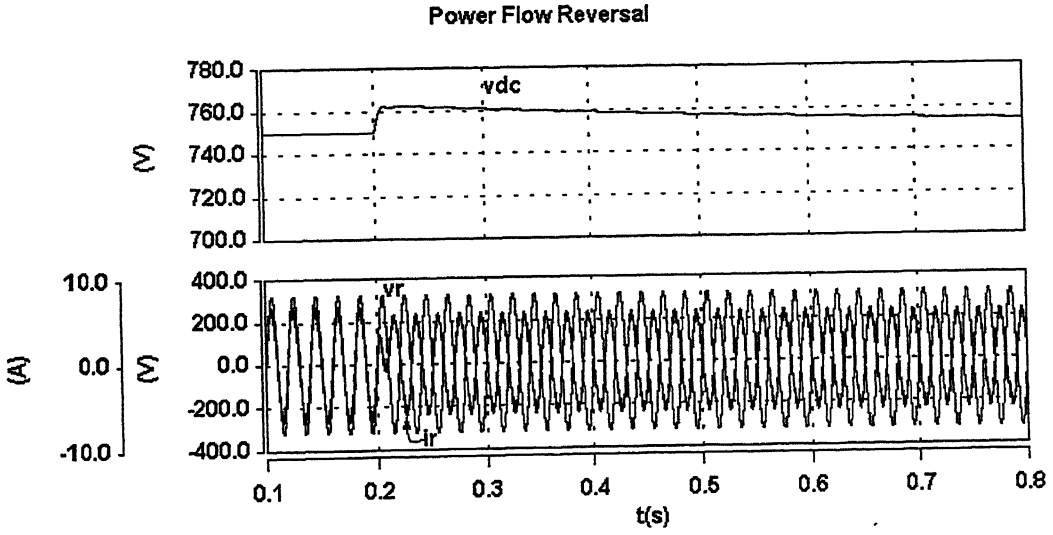


Fig. 3.35 Power flow reversal, rectification to inversion

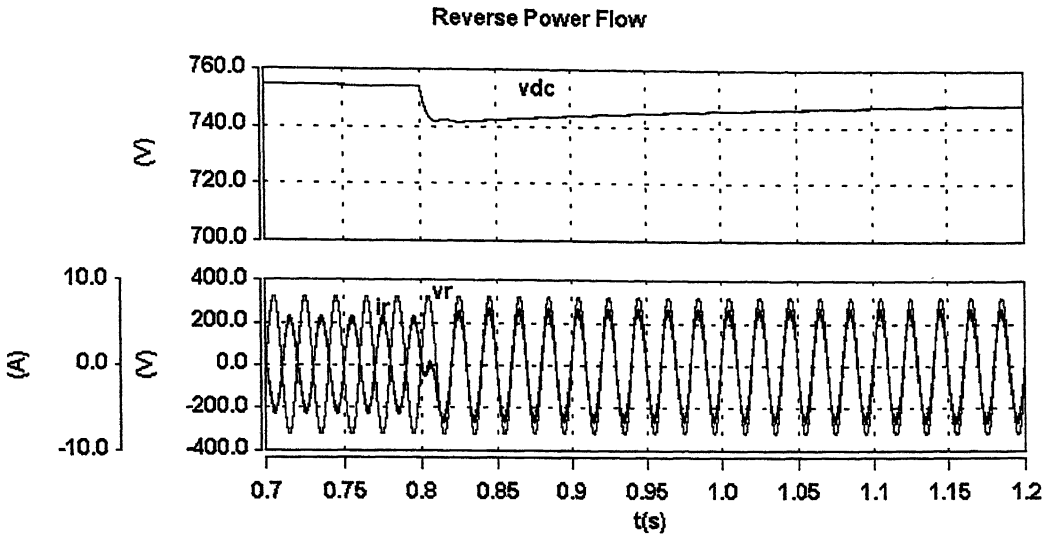


Fig. 3.36 Power flow reversal, inversion to rectification

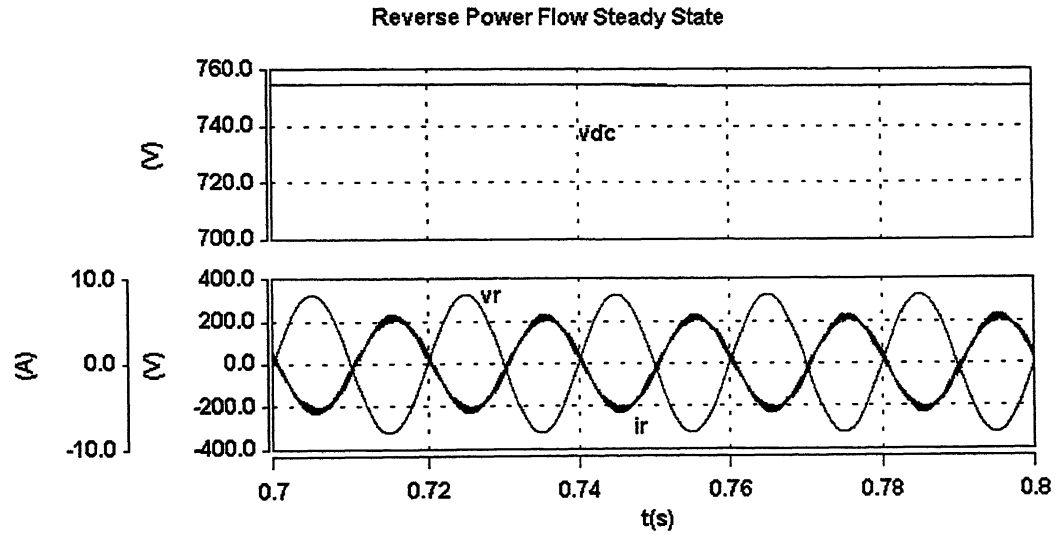


Fig. 3.37 Steady state, reverse power flow condition

3.5 Conclusion

Due to their simple construction, ease of design, capability for bidirectional power flow, reduced input current harmonics and unity power factor operation the Synchronous Link Converters have been used here as the front end converters in ac drives. The SLC acts as the advanced utility interface for the ac drive. Both single and three phase Synchronous Link Converter topologies have been simulated with voltage source inverter-fed induction motor drive. Indirect current control scheme has been used. The simulation results show that the dc link voltage is maintained close to reference value for nominal supply voltage, under the conditions of sag and swell and transitions between them. The input current is in phase with the supply voltage and its harmonic contents are well within acceptable limits.

Chapter – 4

Experimental Realization of the Synchronous Link Converter

4.1 Introduction

In chapter 3, simulation studies have been made for SLC as the advanced utility interface for ac drive system. The experimental realization was done to study the unity power factor operation of Synchronous Link Converter and to study the performance under the conditions of voltage sag, swell and transitions among them. The experimental setup was designed and operated at reduced voltage and power levels. Then simulations were also performed at these levels and the results have been presented for comparison. This chapter gives the details of experimental realization and the simulations.

4.2 Power circuit

The power circuit of the Converter was realized using IGBT switches. The synchronous link converter was fed through a variac. The following components were used in the power circuit.

1. MITSUBISHI CM75DU – 24F IGBT dual power module; 75 A, 1200 V.
2. 0.1 μF, 36.0 Ω Snubber circuit.
3. 22.72 mH Synchronous Link Inductor and 2200 μF dc link capacitor.
4. 50 W load.

4.3 Control circuit

The control circuit (Fig 4.1) is partially realized with analog hardware and partially with computer interface. A high performance data acquisition card, PCL-208, whose details are given in Appendix-B, has been used as an interface between the PC and the external hardware. The dc-link voltage is sensed using a Hall sensor and fed to the computer through the data acquisition card. Using a computer program, the dc link voltage is sensed by the data acquisition card, and the error in dc-link voltage is processed by PI controller. This value is then multiplied with the reactance of synchronous link inductor and sent to the external hardware through D/A channel of PCL-208. The signal is then filtered and multiplied with the phase shifted sine wave using analog multiplier ICL8013 and added with source voltage signal to get the modulating waveform.

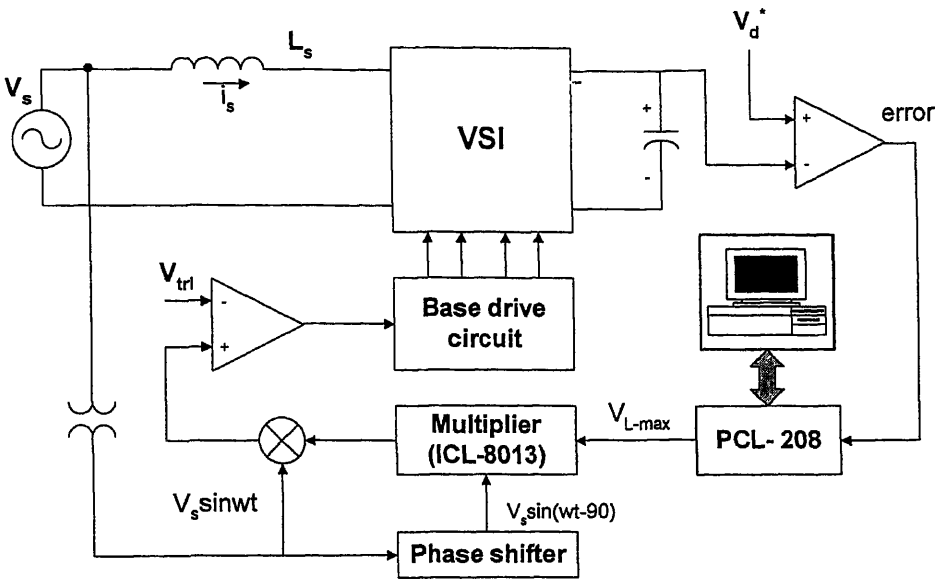


Fig. 4.1Control circuit used in experiment

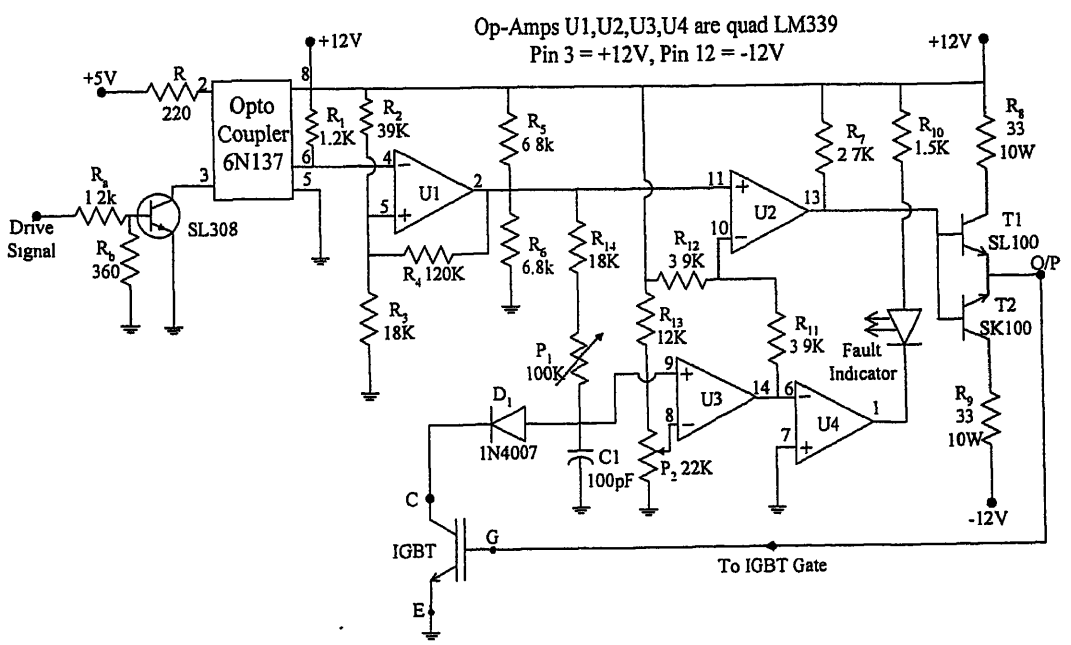


Fig. 4.2 Base drive circuit for IGBT

4.4 Base drive circuit

Fig 4.2 gives the circuit connections of base driver circuit. The function of driver circuit is to provide electrical isolation between the control circuit and power circuit. The electrical isolation is achieved through optocoupler 6N137. The driver circuit also amplifies the low level switching signal coming from the control circuit to the level sufficient to drive the IGBT. Further, the driver circuit provides over current protection by removing signals during fault conditions.

4.5 Simulation and Experimental Results

In this section, the simulation and experimental results of a single phase synchronous link converter operated at nominal voltage, sag and swell conditions are presented. Unity power factor operation is achieved at all the voltages. The simulated results are in good agreement with the experimental results.

The photographs of the experimental set-up are shown in Fig. 4.3. In Figs. 4.4 – 4.11 the source voltage, current and dc link voltage profiles have been shown for nominal voltage condition. The steady state and transient conditions arising out of load variations have also been depicted in these results for simulation as well as experimental setups. The voltage at the ac side of the voltage source inverter of SLC has been shown for full load as well as no load conditions in Figs. 4.10 – 4.11. The harmonic spectrum for the input current has been given in Fig. 4.12. The total harmonic distortion (THD) in the supply current is found to be 4.991%. The supply voltage, current and dc link voltage waveforms, for voltage variation from nominal to sag condition, have been shown in Fig.

4.13 and Fig. 4.14. Figs. 4.15 – 4.18 show the worst case variations for supply voltage that is from 10% swell to 40% sag and vice versa. The source voltage, current and dc link voltage profiles have been presented for these transient conditions. Figs. 4.19 – 4.20 show the steady state condition of voltage sag at full load. The transients under the sag condition due to load variations have been shown in Fig. 4.21 – 4.24.

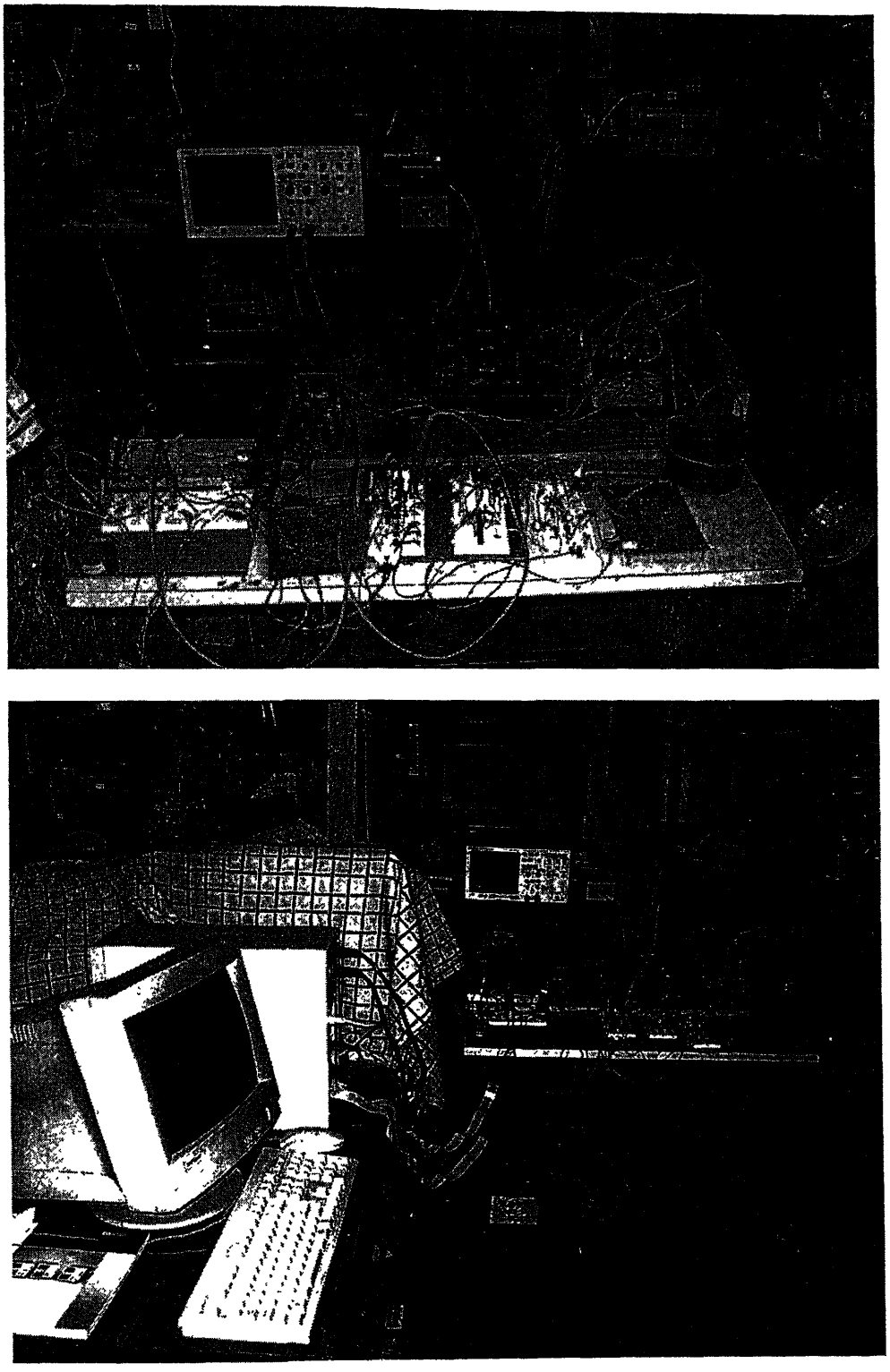
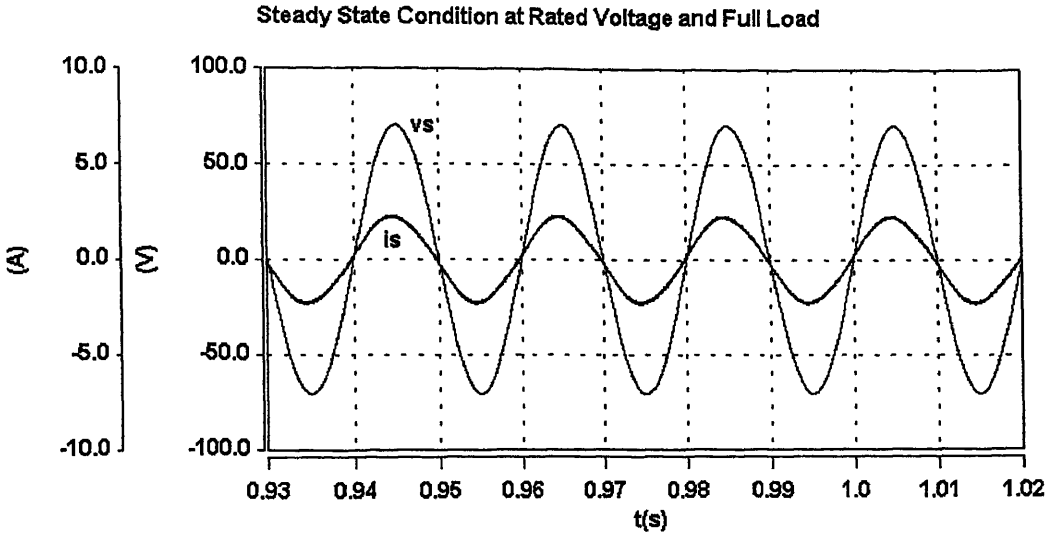
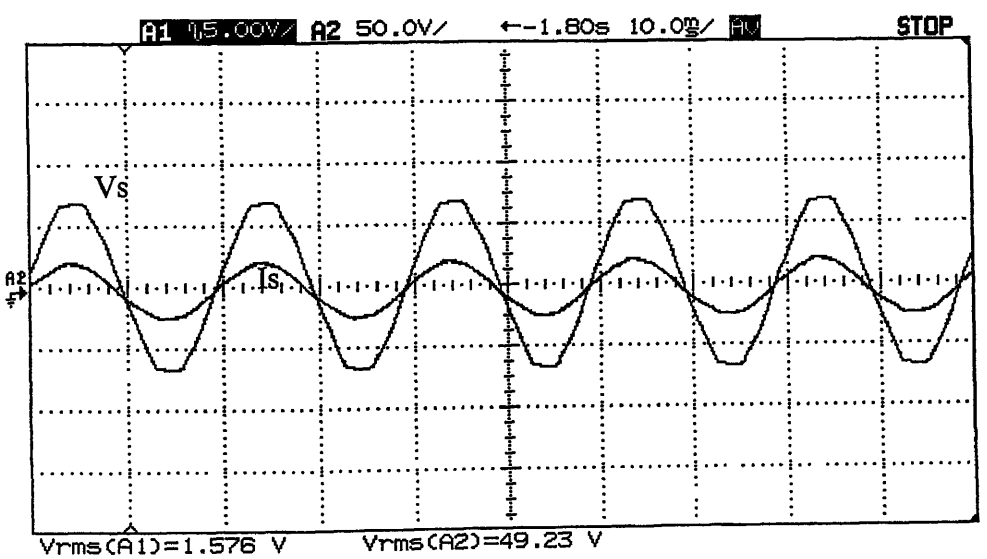


Fig. 4.3 Experimental set up of single stage Synchronous Link Converter



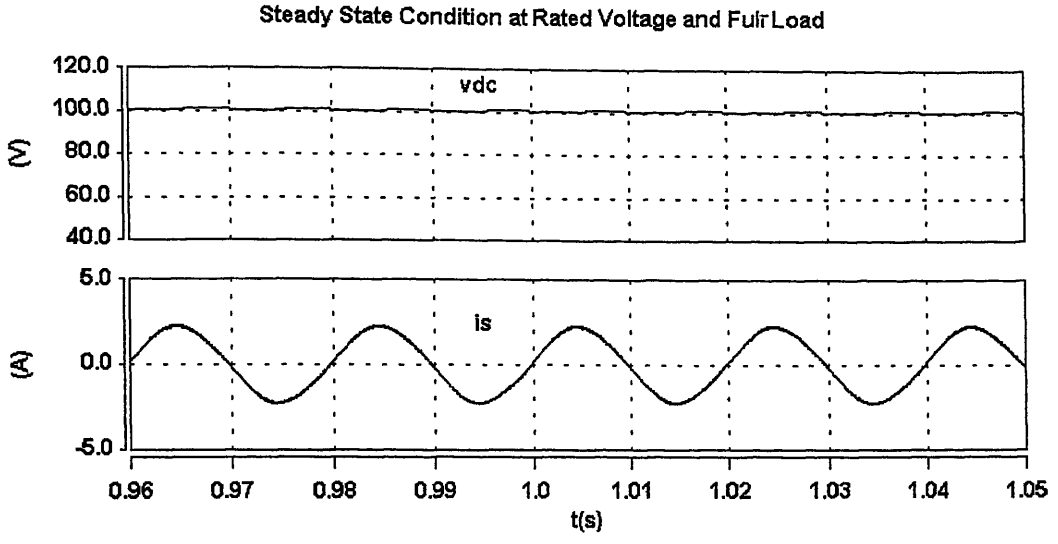
(a) Simulated waveform



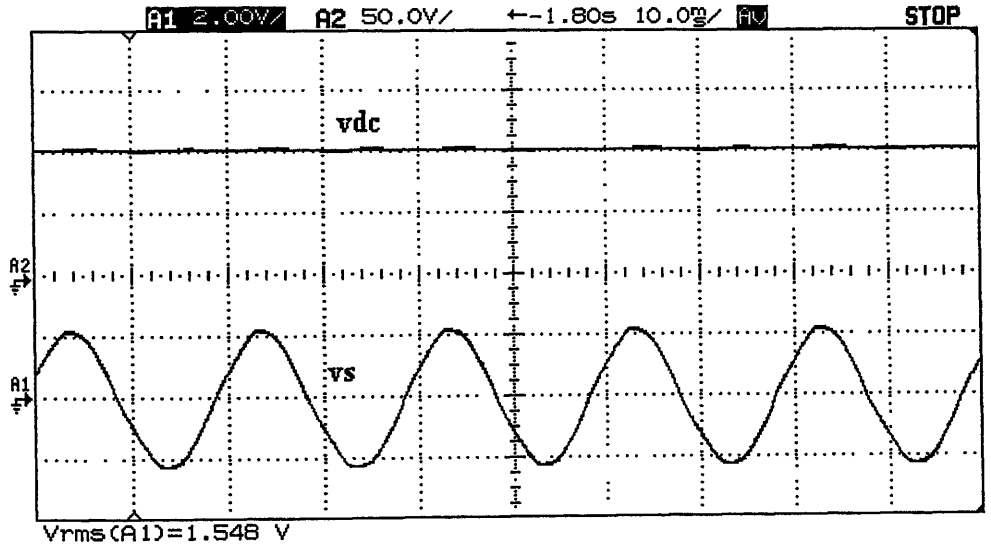
Scale - x-axis:10ms/div, vs: 50 V/div, is: 5 A /div

(b) Experimental waveform

Fig. 4.4 Steady state supply voltage and current at nominal voltage and full load



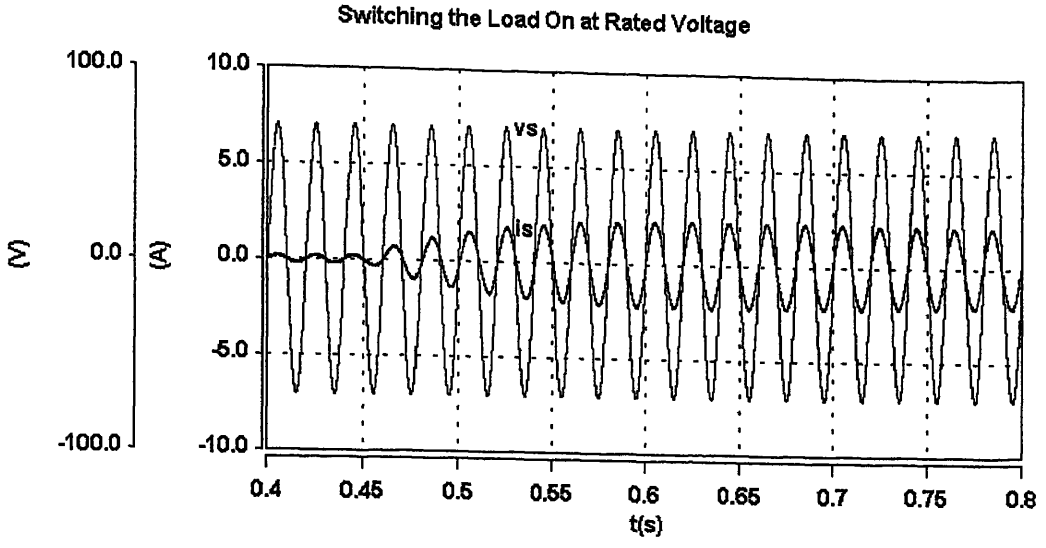
(a) Simulated Waveform.



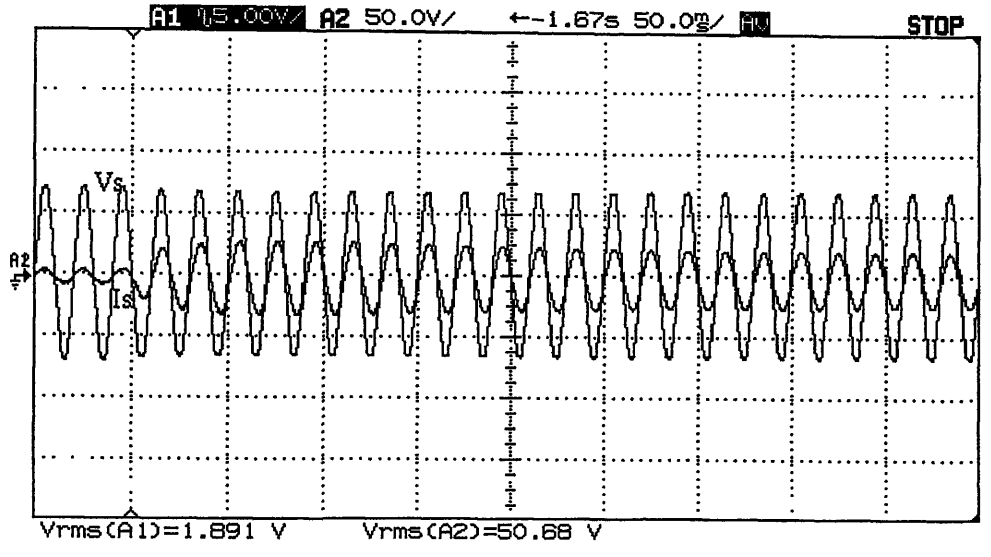
(b) Experimental waveform

Scale - x-axis: 10 ms/div, is: 2 A /div, vdc: 50 V/div

Fig. 4.5 Input supply current and dc link voltage at steady state



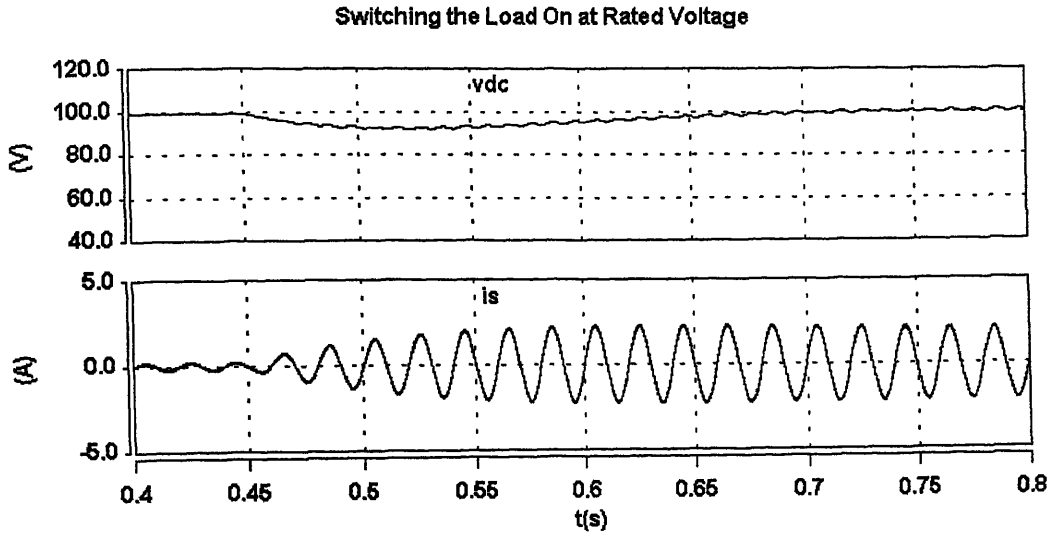
(a) Simulated waveform



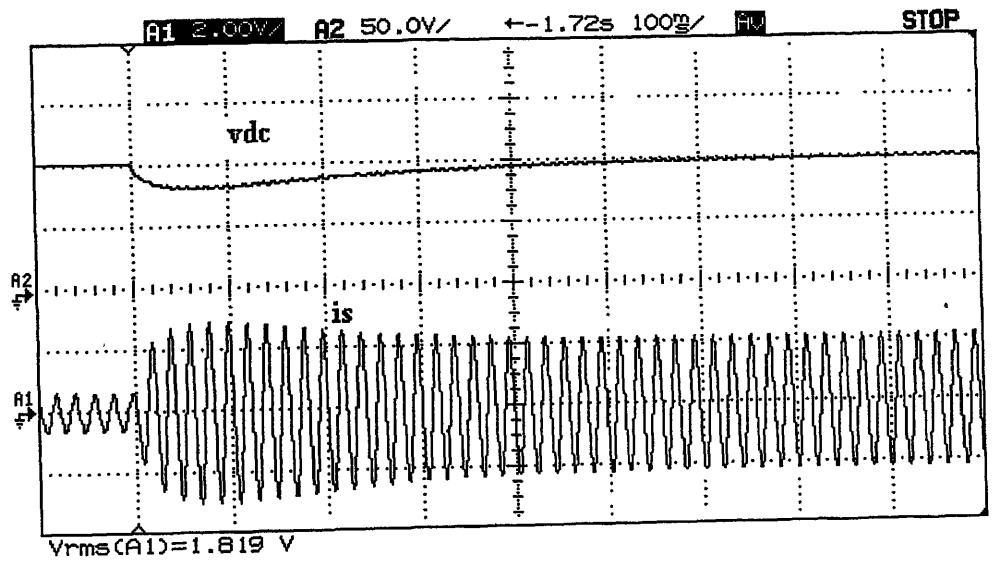
Scale - x-axis: 50ms/div, vs: 50 V/div, is: 5 A/div

(b) Experimental waveform.

Fig. 4.6 Supply voltage and current while switching the load on at rated voltage



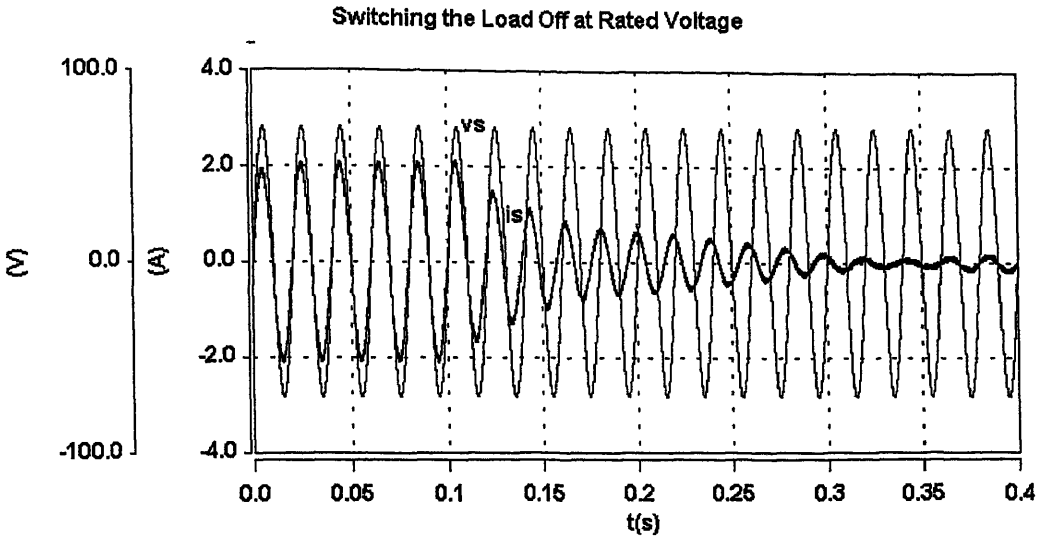
(a) Simulated waveform



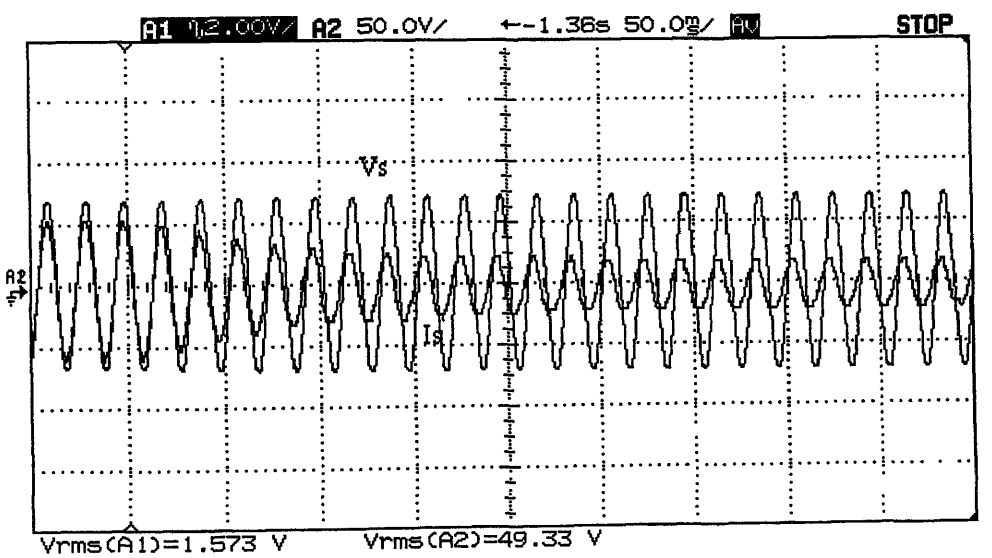
Scale-x-axis: 100 ms/div, vdc: 50 V/div, is: 2 A/div

(b) Experimental waveform

Fig. 4.7 Input supply current and dc link voltage while switching the load on



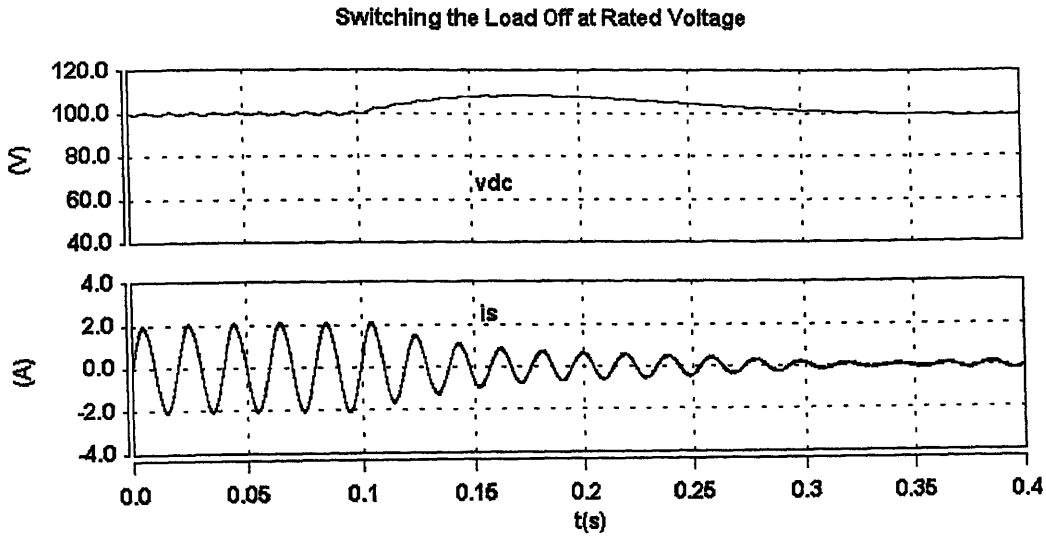
(a) Simulated waveform



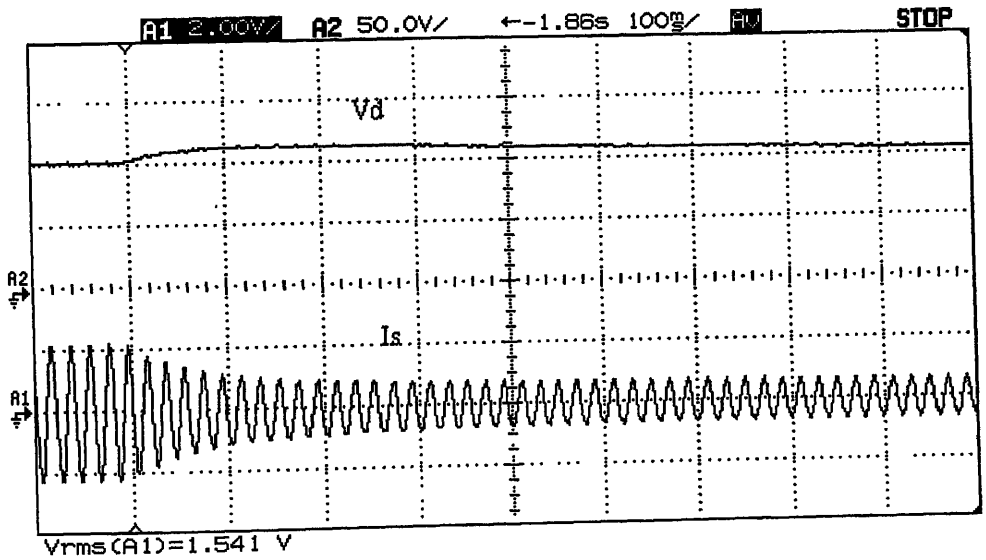
Scale - x-axis: 50 ms/div, vs: 50 V/div, is: 2A/div

(b) Experimental waveform

Fig. 4.8 Supply voltage and current waveforms while switching the load off at nominal voltage



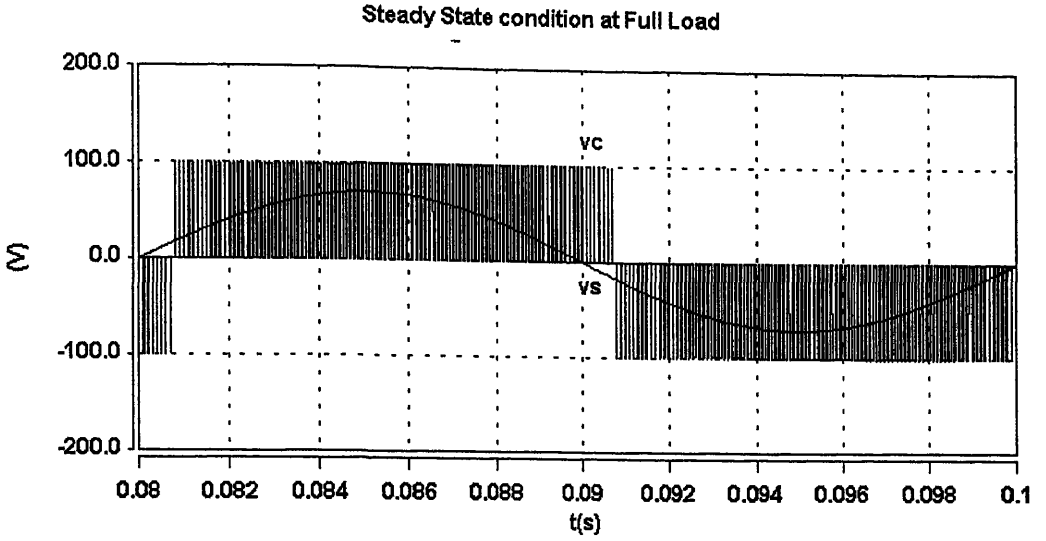
(a) Simulated waveform



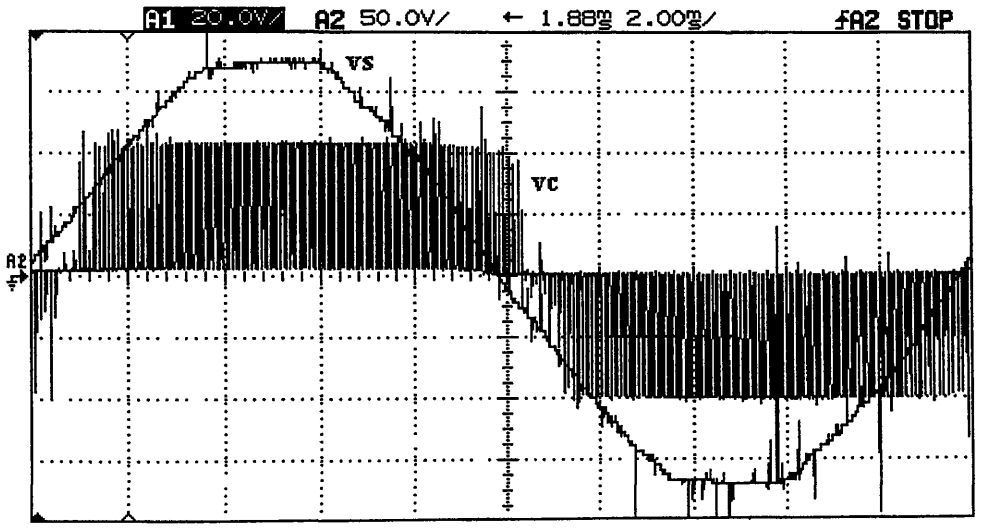
Scale - x-axis: 100 ms/div, vs: 50 V/div, is: 2A/div

(b) Experimental waveform

Fig. 4.9 Supply current and dc link voltage waveforms while switching the load off at rated voltage



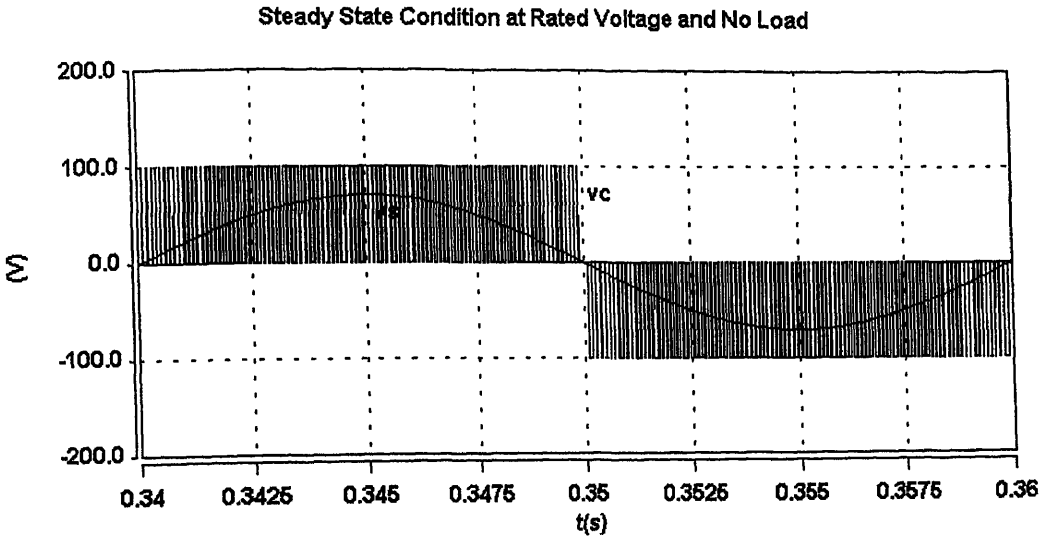
(a) Simulated waveform



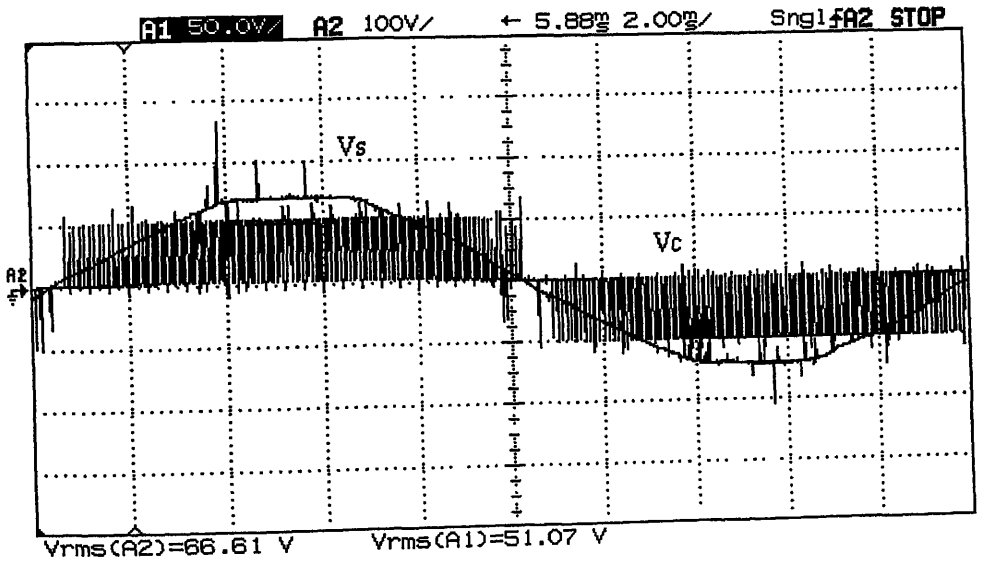
Scale - x-axis: 2 ms/div, vs: 20 V/div, vc: 50 V/div

(b) Experimental waveform

Fig. 4.10 Supply voltage and voltage at the ac side of the voltage source inverter at full load



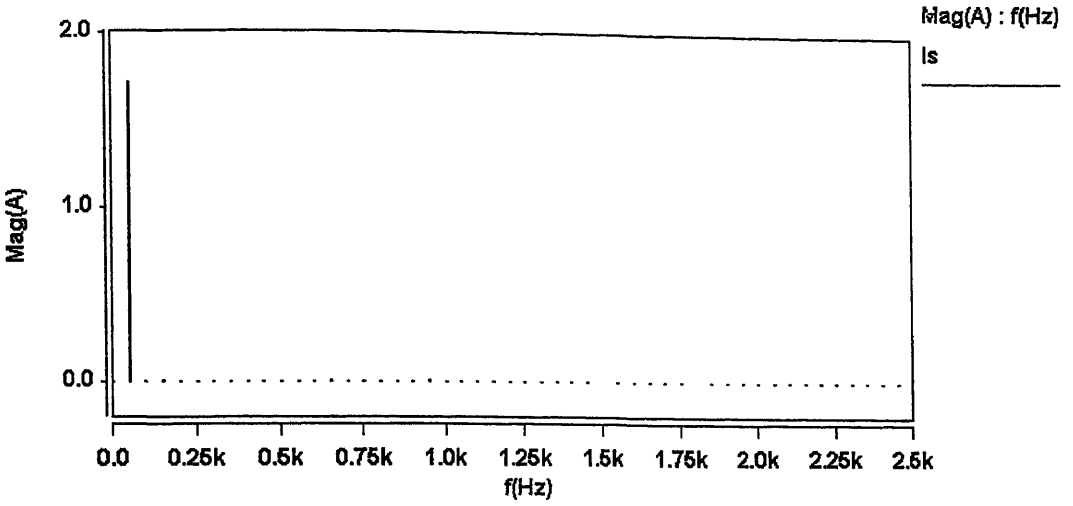
(a) Simulated waveform



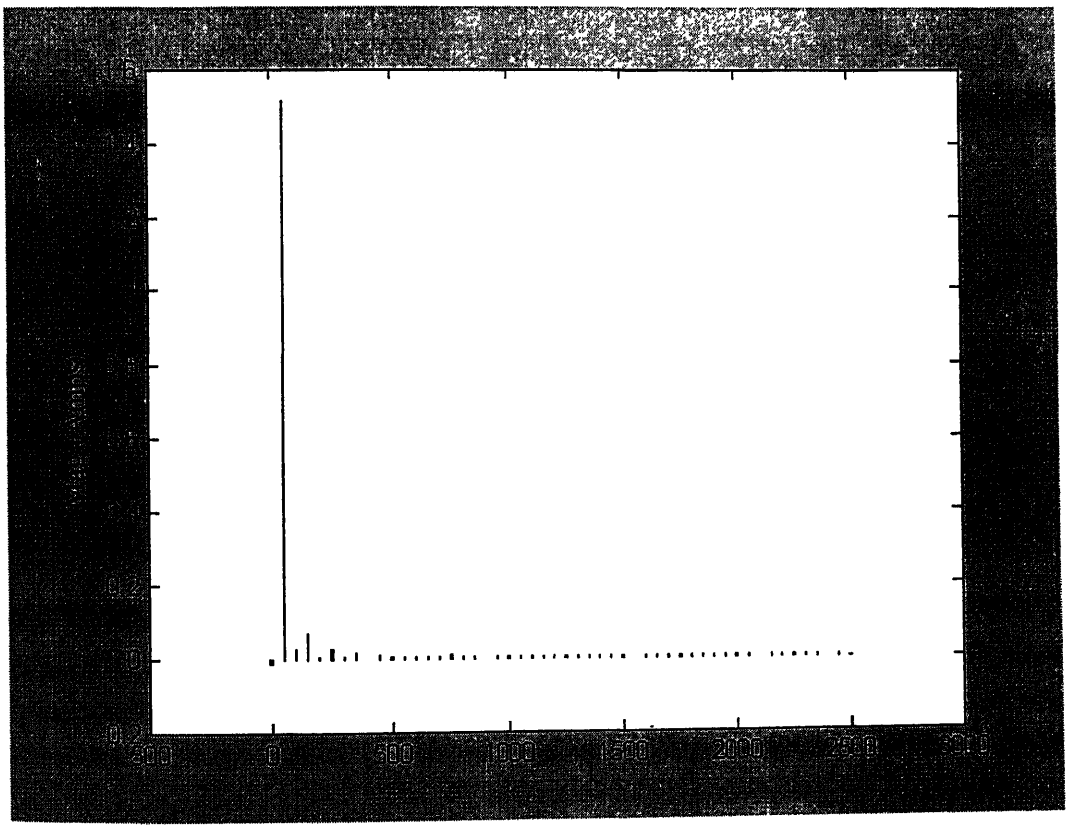
Scale - x-axis: 2 ms/div, vs: 50 V/div, vc: 100 V/div

(b) Experimental waveform

Fig. 4.11 Supply voltage and voltage at the ac side of the voltage source inverter at no load

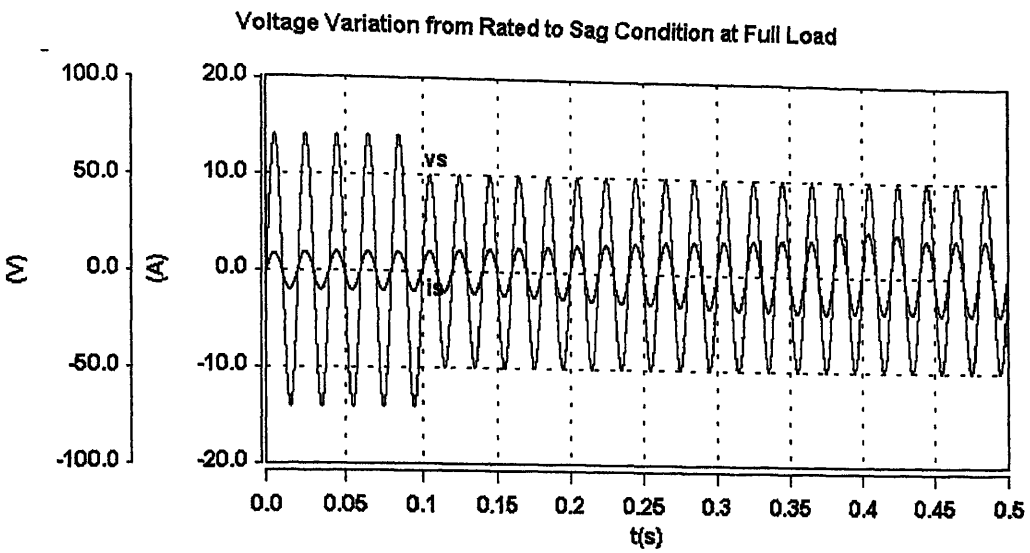


(a) Harmonic spectrum of supply current (Simulated)

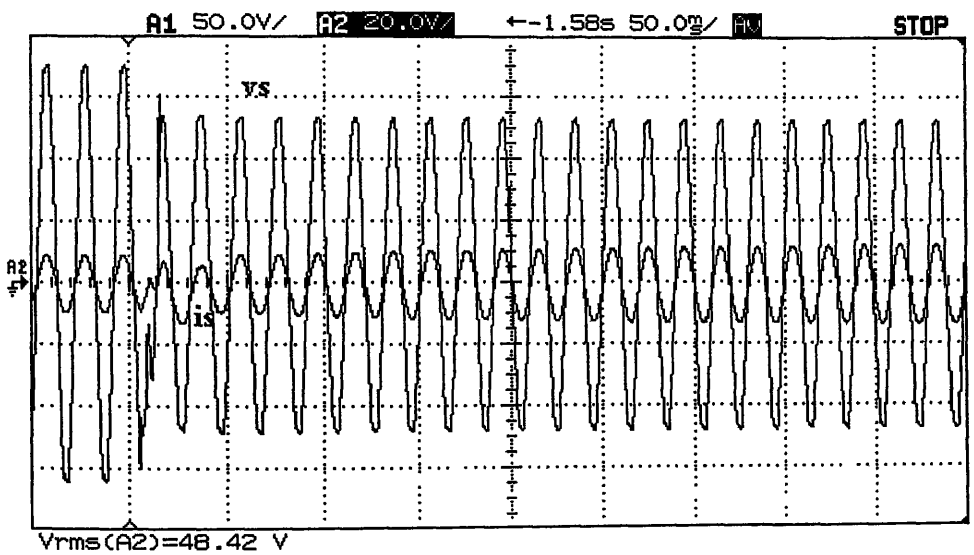


(b) Harmonic spectrum of supply current (Experimental)

Fig. 4.12 Harmonic spectrum of supply current



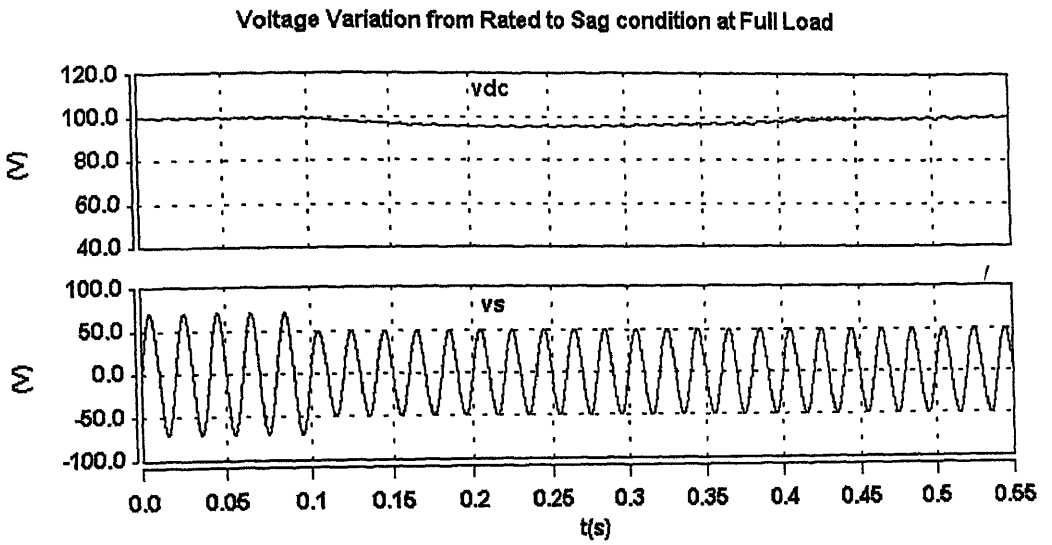
(a) Simulated waveform



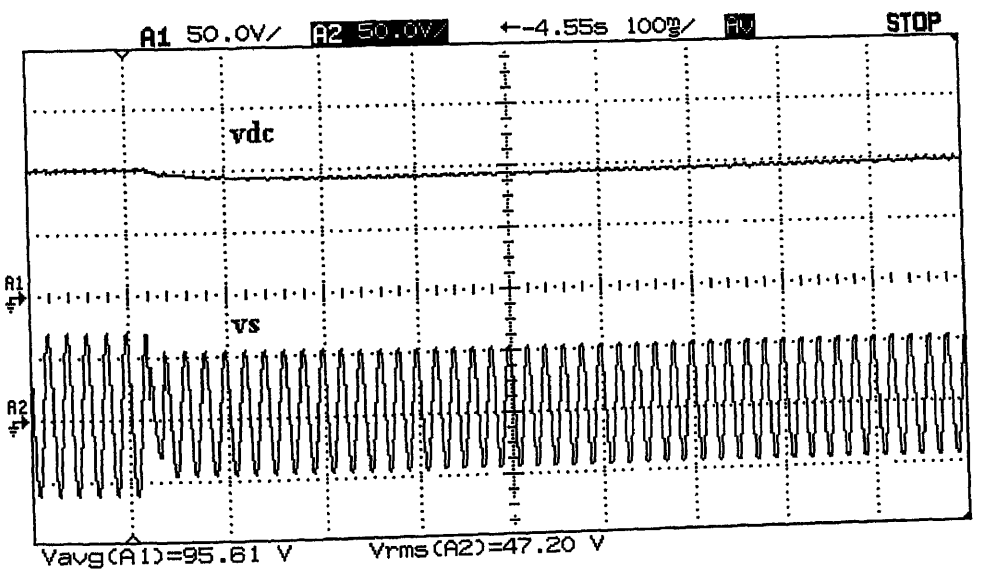
Scale - x-axis: 50 ms/div, vs: 20 V/div, is: 5 A/div

(b) Experimental waveform

Fig. 4.13 Supply voltage and current for voltage variation from rated to sag condition at full load



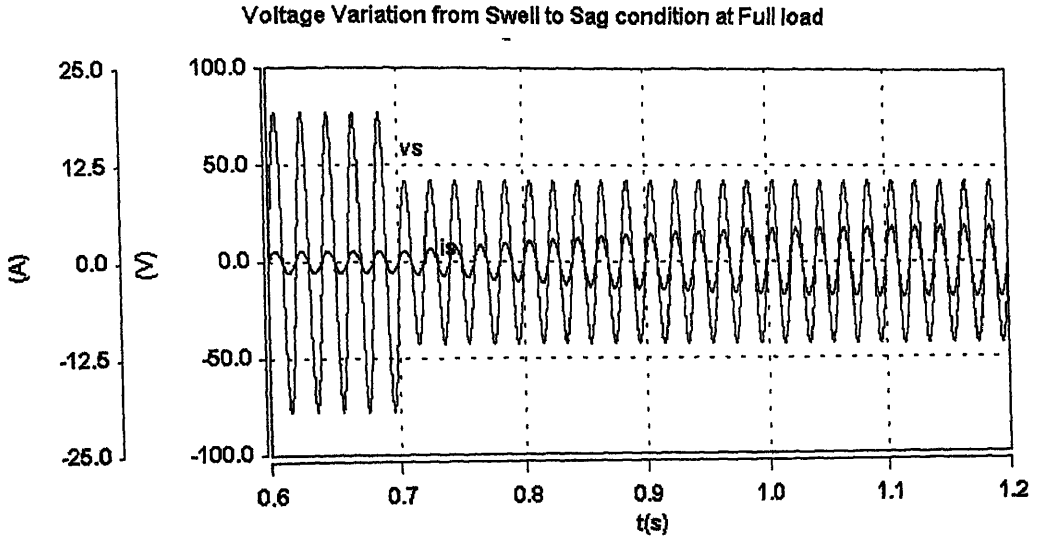
(a) Simulated waveform



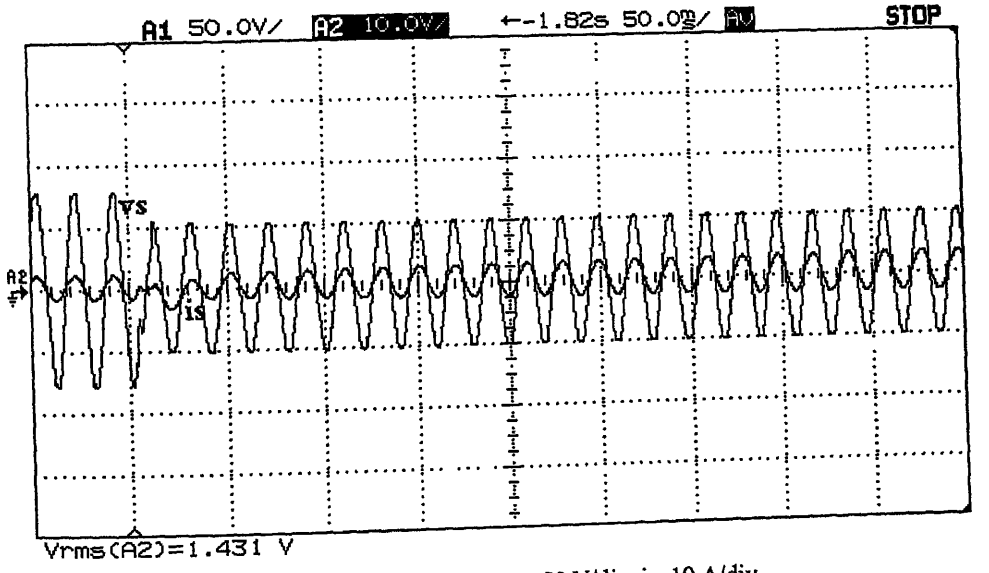
Scale - x-axis: 100 ms/div, vs: 50 V/div, vdc: 50 V/div

(b) Experimental waveform

Fig. 4.14 Supply voltage and dc link voltage for voltage variation from rated to sag condition at full load



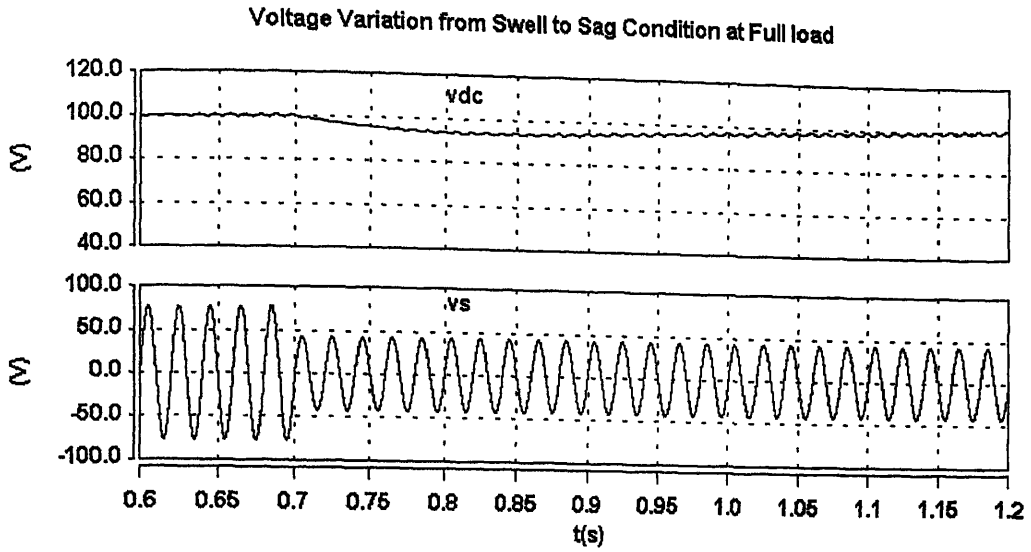
(a) Simulated waveform



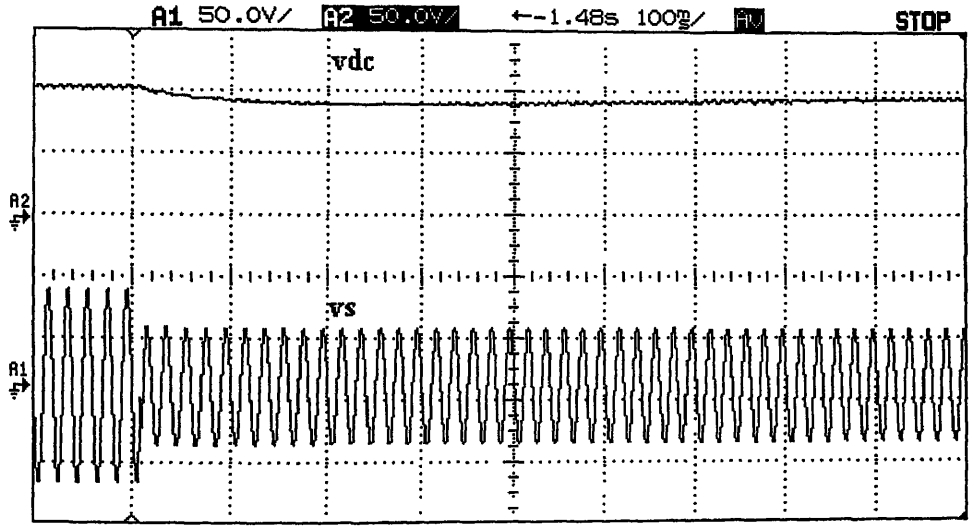
Scale - x-axis: 50 ms/div, vs: 50 V/div, is: 10 A/div

(b) Experimental waveform

Fig. 4.15 Supply voltage and current for voltage variation from swell to sag condition at full load



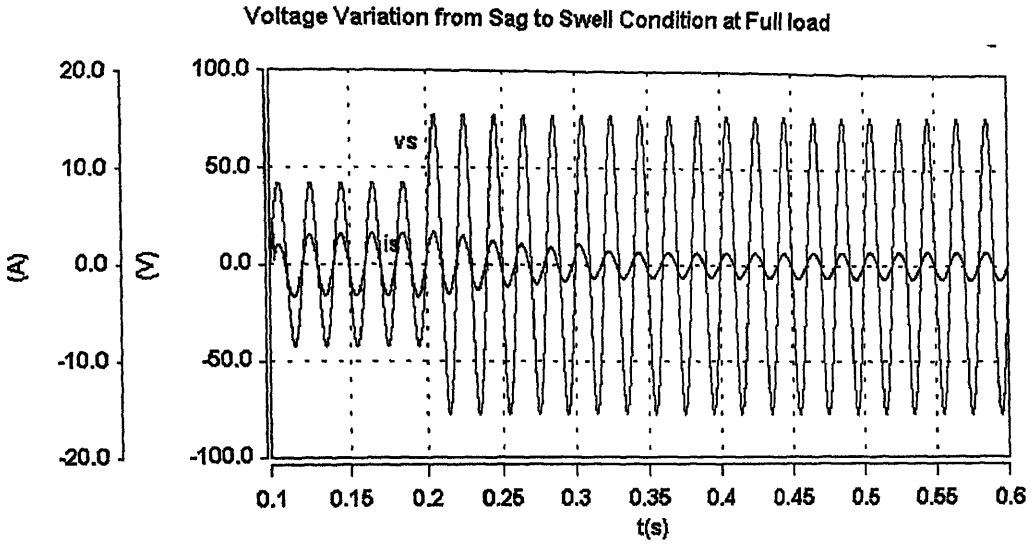
(a) Simulated waveform



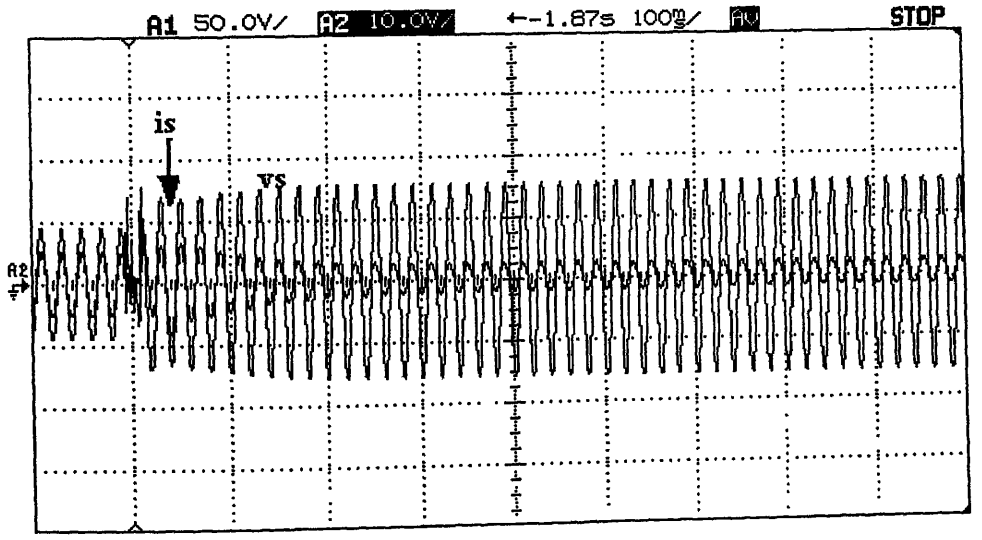
Scale - x-axis: 50 ms/div, vs: 50 V/div, vdc: 50 V/div

(b) Experimental waveform

Fig. 4.16 Supply and dc link voltage for variation of voltage from swell to sag condition at full load



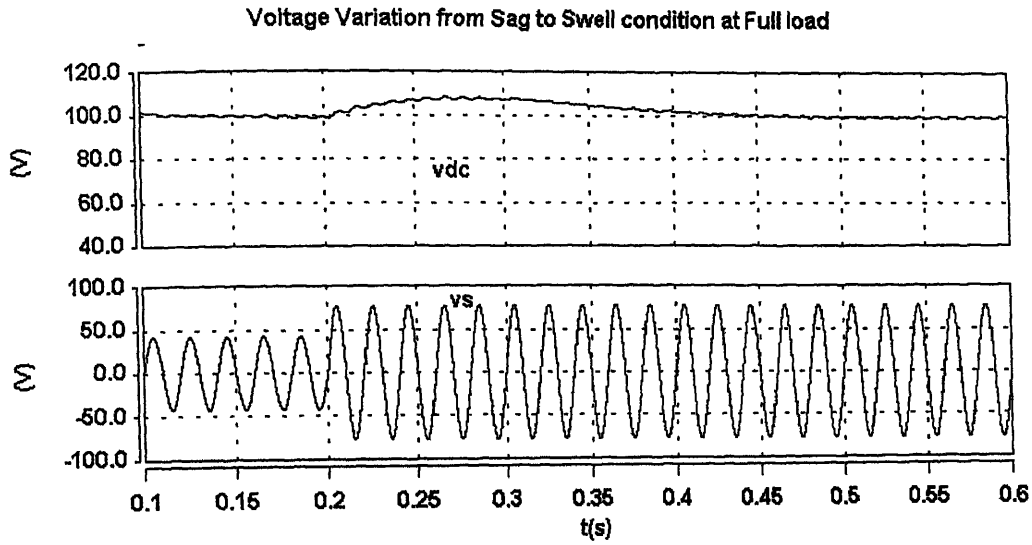
(a) Simulated waveform



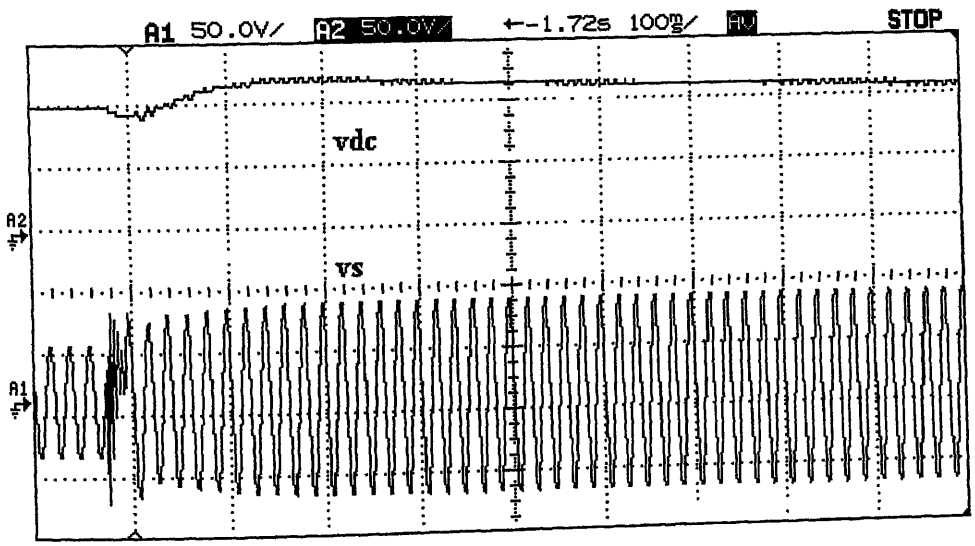
Scale - x-axis: 100 ms/div, vs: 50 V/div, is: 10 A/div

(b) Experimental waveform

Fig. 4.17 Supply voltage and current for variation of voltage from sag to swell condition at full load



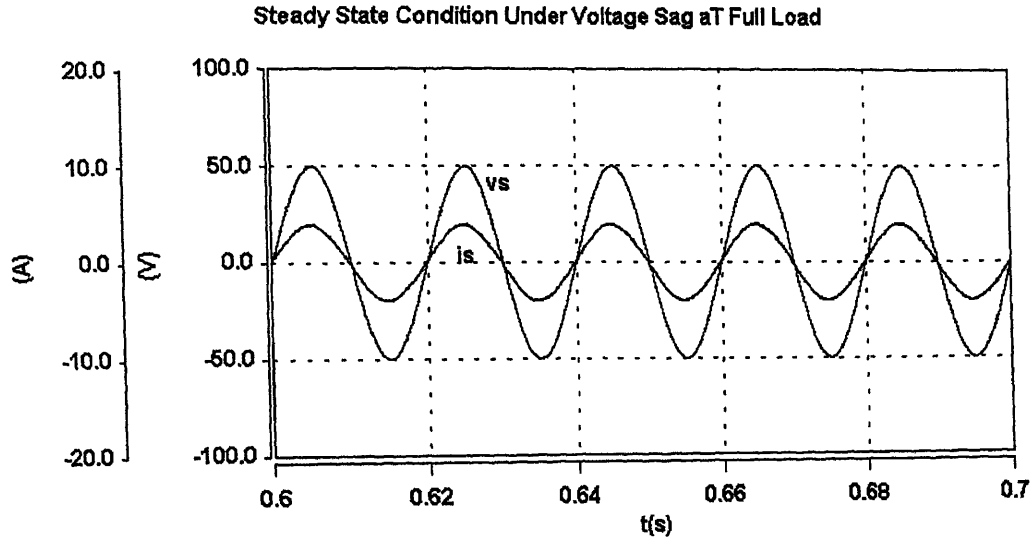
(a) simulated waveform



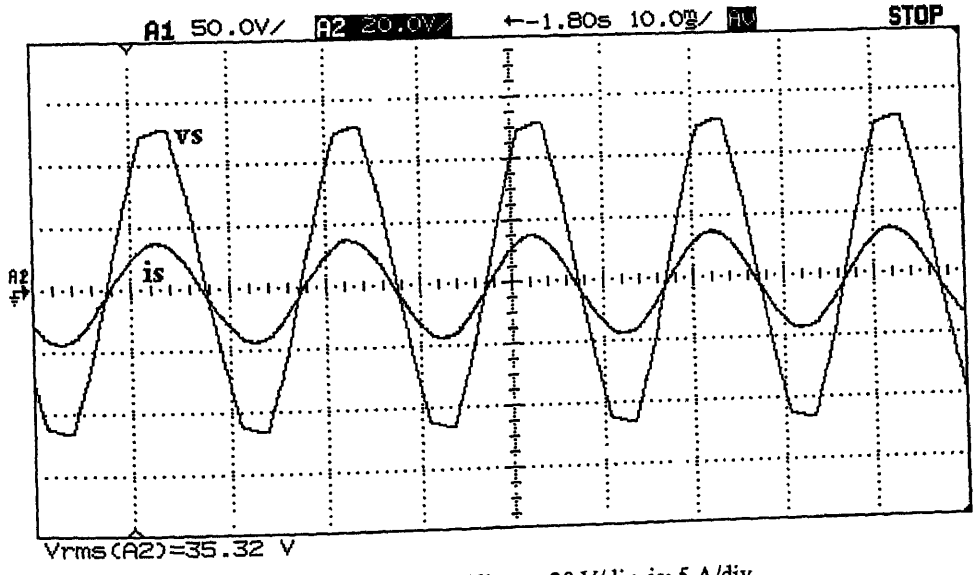
Scale - x-axis: 100 ms/div, vs: 50 V/div, vdc: 50 V/div

(b) Experimental waveform

Fig. 4.18 Supply and dc link voltage for variation of voltage from sag to swell condition at full load



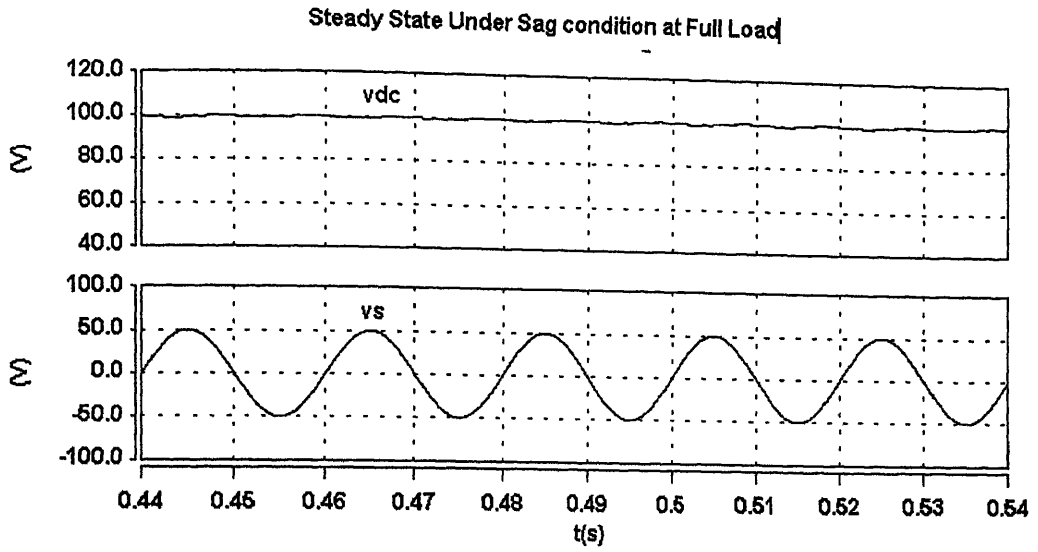
(a) Simulated waveform



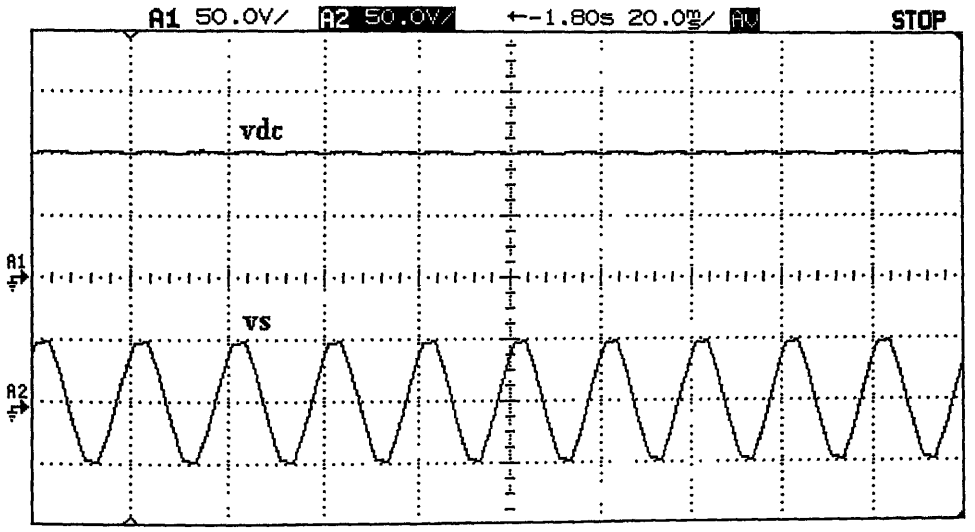
Scale - x-axis: 10 ms/div, vs: 20 V/div, is: 5 A/div

(b) Experimental waveform

Fig. 4.19 Supply voltage and current in steady state condition under voltage sag at full load



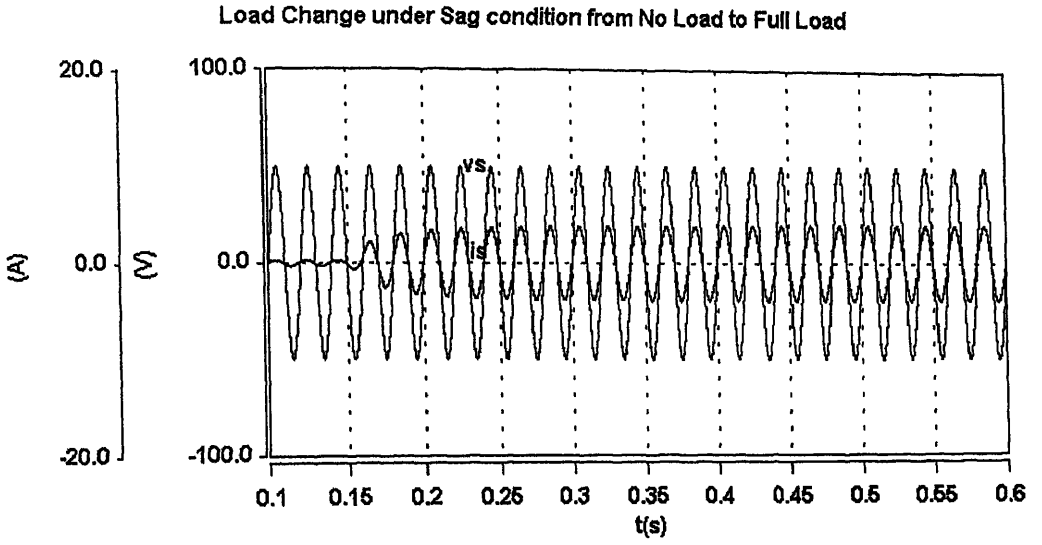
(a) Simulated waveform



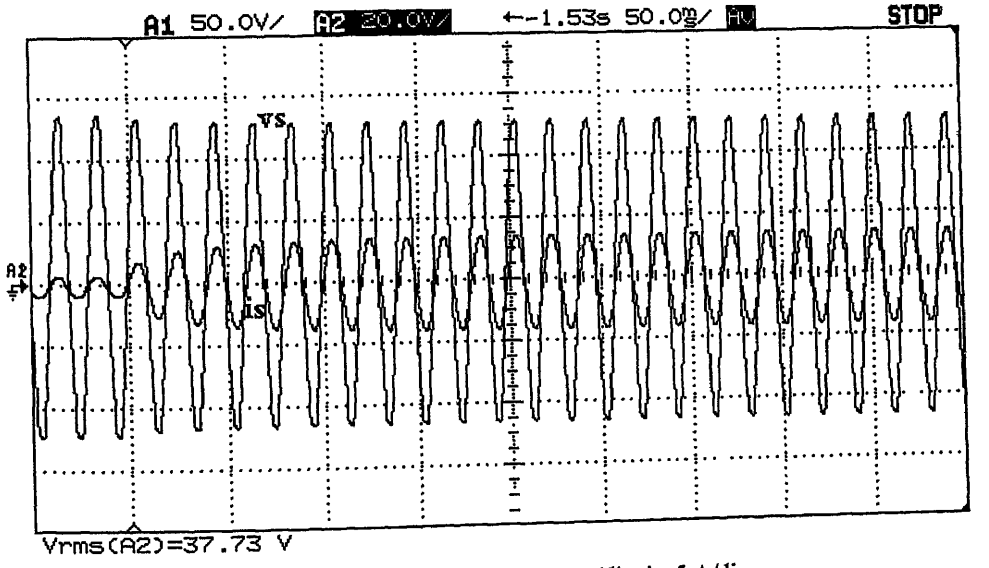
Scale - x-axis: 20 ms/div, vs: 50 V/div, vdc: 50 V/div

(b) Experimental waveform

Fig. 4.20 Supply voltage and dc link voltage under voltage sag condition at full load



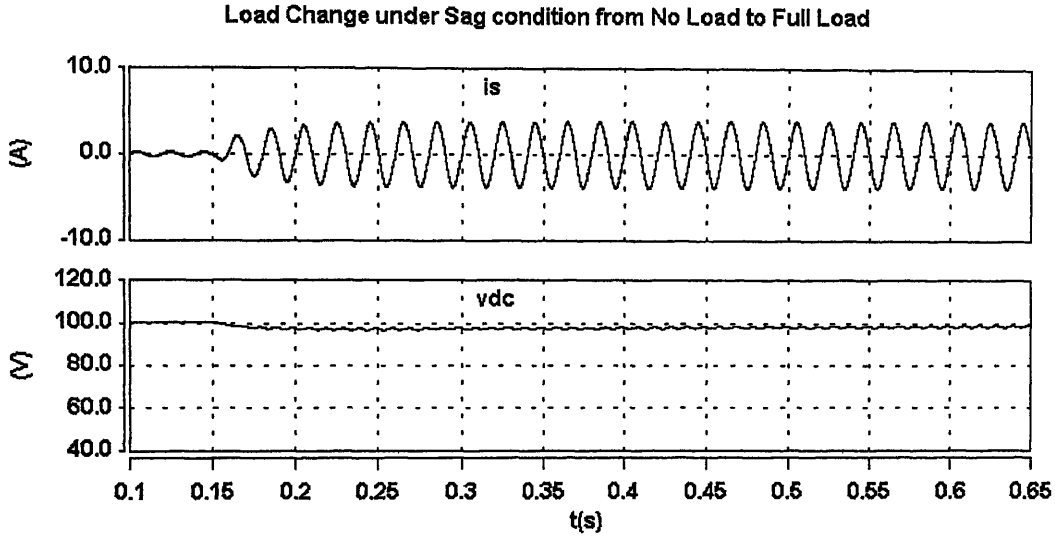
(a) Simulated Waveform



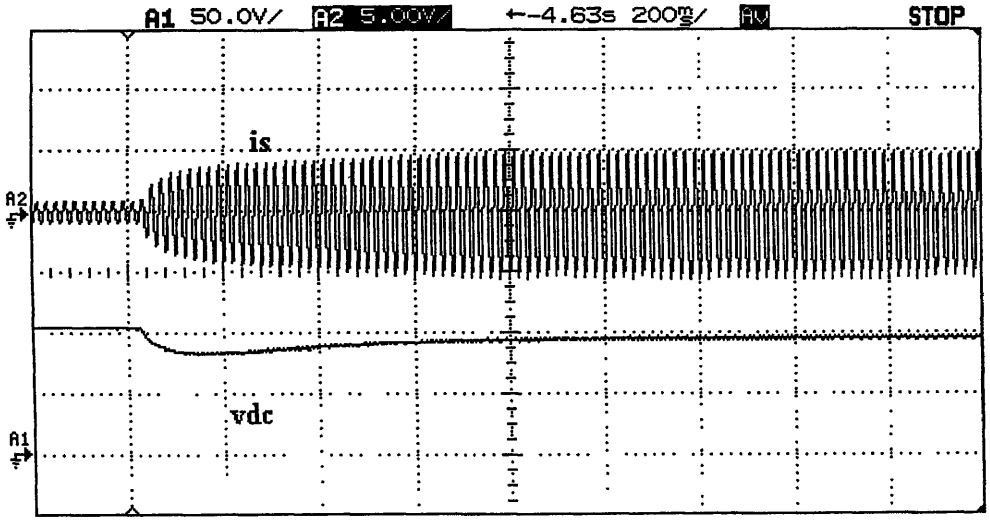
Scale - x-axis: 50 ms/div, vs: 20 V/div, is: 5 A/div

(b) Experimental waveform

Fig. 4.21 Supply voltage and current under voltage sag condition while load is switched on



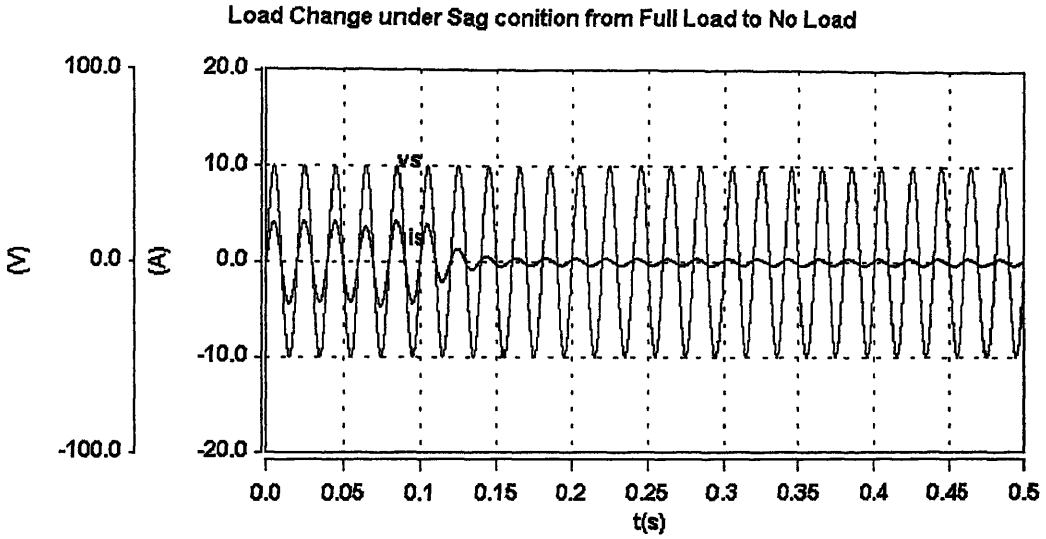
(a) Simulated Waveform



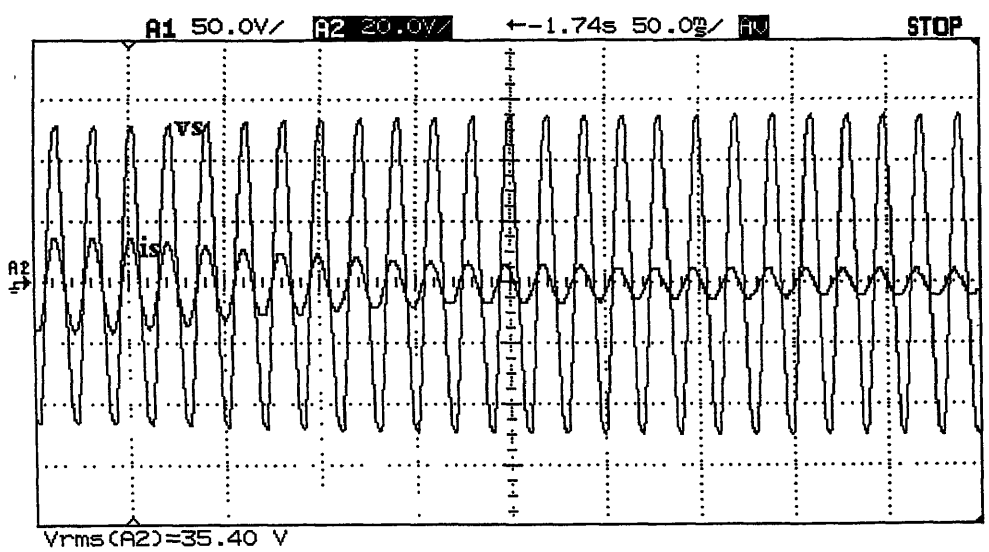
Scale - x-axis: 200 ms/div, is: 5 A/div, vdc: 50 V/div

(b) Experimental waveform

Fig. 4.22 Supply current and dc link voltage under voltage sag condition while load is switched on



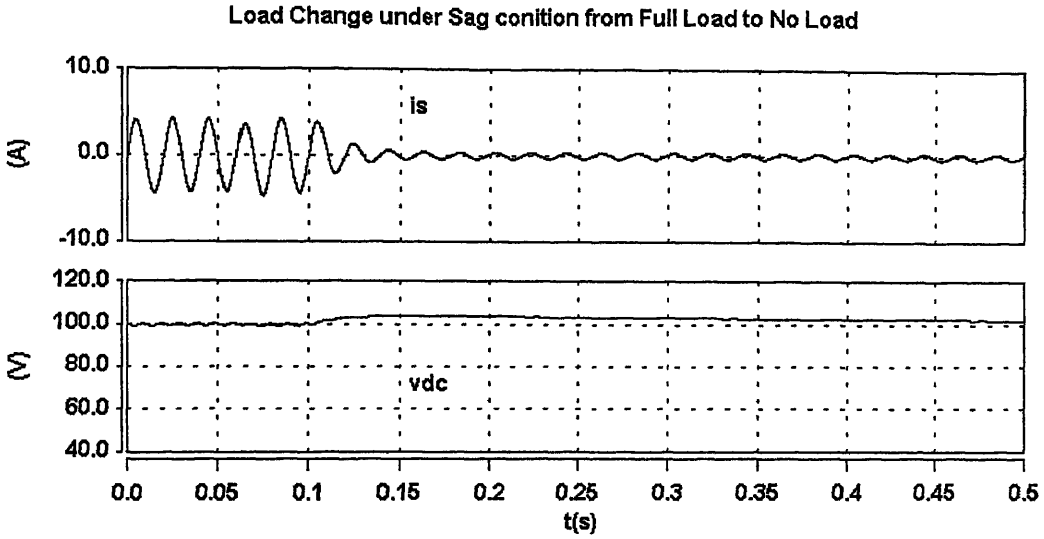
(a) Simulated Waveform



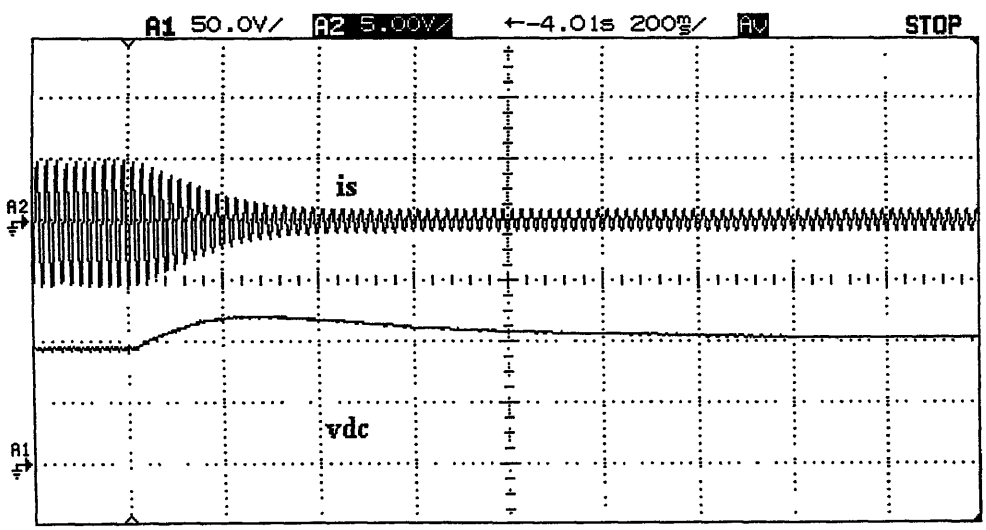
Scale - x-axis: 50 ms/div, vs: 20 V/div, is: 5 A/div

(b) Experimental waveform

Fig. 4.23 Supply voltage and current under voltage sag condition while load is switched off



(a) Simulated waveform



Scale - x-axis: 200 ms/div, is: 5 A/div, vdc: 50 V/div

(b) Experimental waveform

Fig. 4.24 Input current and dc link voltage under voltage sag condition while load is switched off

4.6 Conclusion

The experimental set-up has been explained in this chapter. Details of control circuits are also given. The simulation and experimental results have been compared and they agree satisfactorily. The important observations are that the dc link voltage is maintained close to the reference value under voltage sag, voltage swell and load variations. Further, the source current is almost sinusoidal and in phase with the source voltage. The total THD in source current under steady state is observed to be 4.991%.

Chapter – 5

Conclusions

5.1 Conclusions

The nuisance tripping of ac drives, proliferation of voltage sensitive loads, due to occurrence of frequent voltage sags, and the consequent costly down times have forced researchers to come up with methods to provide voltage sag ride-through capability to the adjustable speed ac drives. The restrictions on harmonics generated by loads have made it mandatory to have advanced utility interface, which can draw sinusoidal current.

In this dissertation such an advanced utility interface has been developed. An advanced converter topology, called Synchronous Link Converter, has been used as the front end converter for the ac drive system. Indirect current control scheme has been used which, being a constant switching frequency scheme, is suitable for high power

applications too. By proper designing of the synchronous link inductor, the input supply current harmonics are maintained within acceptable limits. The dc link voltage is maintained close to the reference even under the conditions of supply voltage sag, swell and load variations etc. Thus, the drive can run unaffected by the supply voltage variations up-to the designed limit at full load. At the same time, the current drawn from supply is at unity power factor. Experimental realization of the synchronous link converter was materialized with PC interfacing for closed loop control. The effectiveness of the proposed utility interface, for voltage sag ride-through capability and drawing unity power factor sinusoidal current from supply, has been demonstrated through extensive simulation and experimental results.

The main contributions of the present thesis can be summarized as follows:

1. Design, analysis, simulation and implementation of Synchronous link converter as the front end converter for ac drive system, working as the advanced utility interface.
2. Development of a working model of the synchronous link converter with voltage sag ride through capability, for a resistive load, in the laboratory.
3. Experimental validation of the simulation results.

5.2 Scope for the future work

The following are the possible scope for future work.

1. Energy storage systems can also be incorporated into the system so as to have ride-through capability for short duration voltage interruptions also.

2. Development of mathematical model of the complete drive system and the design of controller based on mathematical model can be done.
3. The PC can be replaced by a Microprocessor / DSP controller for industrial application.

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Appendix-A

Voltage and Current Sensor Specifications

A-1 Voltage Sensor

PCB Mounting Hall Effect Voltage Transducer (Model LV 25-P)

Technical Specifications:

Nominal current I_N	:	10 mA
Nominal analogue output current	:	25 mA
Turns ratio	:	2500:1000
Overall accuracy at 25°C	:	± 0.6% of I_N
Supply Voltage	:	± 15 V (± 5%)
Isolation	:	2.5 kV (rms)/50 Hz/1 min
Linearity	:	< 0.2%
Response time	:	< 40 μ s for R1 series 25 kΩ resistor
Operating temperature	:	0°C to 70°C
Current Consumption	:	10 mA + output current
Primary internal resistance	:	250 Ω (at 70°C)
Secondary internal resistance	:	110 Ω (at 70°C)
Weight	:	22 gm
Operating range	:	10 to 500 V

Polarity marking : A positive output current is obtained on terminal M when a positive voltage is applied on terminal +HT of the primary circuit.

Primary resistor R_1 : The transducer's optimum accuracy is obtained with the nominal primary current. As for as possible, R1 should be calculated so that the nominal voltage to be measured corresponds to a primary current of 10 mA.

Measuring resistance		R_M min.	R_M max.
with ± 15 V	at ± 10 mA max.	100 Ω	350 Ω
	at ± 14 mA max.	100 Ω	190 Ω

Connection pins

Pin + : Supply voltage +15 V

Pin M : Measuring point

Pin - : Supply voltage -15 V

Pin + HT : Primary voltage +

Pin - HT : Primary voltage -

A-2 Current Sensor

LEM Module LA 55-P

This current transducer can be used for electronic measurement of currents: DC, AC, IMPL., etc., with galvanic isolation between the primary (high power) and the secondary (electronic) circuits.

Electrical Data

Nominal current IN : 50 A

Measuring Range : 0 to ± 70 A at 70°C

Measuring resistance		: at + 70°C		at + 85°C	
		R_M min.	R_M max.	R_M min	R_M max.
With ± 12 V	at ± 50 A max.	10 Ω	100 Ω	60 Ω	95 Ω
	at ± 70 A max.	10 Ω	50 Ω	60 Ω	60 Ω
With ± 15 V	at ± 50 A max.	50 Ω	160 Ω	135 Ω	155 Ω
	at ± 70 A max.	50 Ω	90 Ω	135 Ω	135 Ω

Nominal analog output current : 50 mA

Turns ratio : 1:1000

Accuracy at +25°C and at ± 15 V (± 5 %) : ±0.65 % of I_N

Accuracy at +25°C and at ± 12 V to ± 15 V	:	±0.9 % of I_N
Supply voltage	:	+ and - 12 to 15 V (± 5 %)
Isolation between primary and secondary	:	2 kV rms/50 Hz/1 min.

Accuracy-Dynamic performance

Zero offset current at ± 25°C	: max. ± 0.2 mA	
Residual current after an overload of 3x I_N	: max. ± 0.3 mA	
Thermal drift of offset current		
(between 0°C and +70°C)	: typical ± 0.1 mA	max. ± 0.5
mA		
(between -25°C and +85°C)	: typical ± 0.1 mA	max. ± 0.6
mA		
Linearity	: better than 0.15%	
Response time	: inferior at 500 nS	
Rise time	: better than 1 μs	
di/dt accuracy followed	: better than 200 A/μs	
Band width	: 0 to 200 kHz (-1dB)	

General Data

Operating temperature	: -25°C to +85°C
Storage temperature	: -40°C to +90°C
Current consumption	: 10 mA (at ± 15 V) + output current
Secondary internal resistance	: 80 Ω (at +70°C), 85 Ω (at +85°C)
Weight	: 18 gm

Appendix-B

Specifications of PCL – 208 Data Acquisition card

PCL – 208 is a high performance, high speed, multifunction data acquisition card for the IBM PC/XT/AT or compatibles. The high end specifications of this full size card and complete software support make it ideal for wide range of applications in the industrial and laboratory environment, like data acquisition, process control, automatic testing and factory automation.

Main features:

- Switch selectable 16 single – ended or 8 differential analog input channels.
- An industrial standard 12 Bit successive approximation converter (ADC674) to convert analog inputs. The maximum A/D sampling rate is 60 kHz in DMA mode.
- Switch selectable versatile analog input ranges.

  Bipolar: +/- 0.5 V, +/- 1 V, +/- 2.5 V, +/- 5 V, +/- 10 V.

  Unipolar: +1V, +2 V, +5 V, +10 V.
- Provides three A/D trigger modes: software trigger, Programmable pacer t rigger and external trigger pulse trigger.
- A/D converted data can be transferred by program control, interrupt handler routine or DMA transfer.
- An INTEL 8254 Programmable Timer/ Counter provides pacer output (trigger pulse) at the rate of 2.5 MHz to 71 minutes / pulse to the A/D. The timer time

base is switch selectable 10 MHz or 1 MHz. One 16 – bit counter channel is reserved for user configuration applications.

- Two 12 bit monolithic multiplying D/A output channels. Output range of 0 to +5V can be created by using the onboard -5 V reference. This precision reference is derived from the A/D converter reference. External AC or DC reference can also be used to generate other D/A output ranges.
- TTL/DTL compatible 16 digital input & 16 digital output channels.

A/D & D/A converter Specifications

Analog Input Specifications:

Channels	:	16 Single-ended or 8 Differential, switch selectable.
Resolution	:	12 bits.
Input Range	:	Unipolar: +1 V, +2 V, +5 V, +10 V. Bipolar: +/- 0.5 V, +/- 1 V, +/- 2.5 V, +/- 5 V, +/- 10 V. All input ranges are switch selectable.
Over voltage	:	Continuous +/- 30 V Max.
Conversion Type	:	Successive Approximation.
Conversion Speed	:	60 kHz max.
Accuracy speed	:	0.01% of reading +/- 1 bit.
Linearity	:	+/- 1 bit.
Trigger Mode	:	Software trigger, onboard programmable timer or external trigger.
Data transfer	:	Program control, Interrupt control or DMA.

Analog Output Specifications:

Channels	:	2 channels.
Resolution	:	12 bits.
Output Range	:	0 to +5 V with fixed -5 V reference.
		+/- 10 V with external DC or AC reference.
Reference Voltage	:	Internal: -5V (+/- 0.05 V).
		External: DC or AC, +/- 10 V max.
Conversion Type	:	12 bit monolithic multiplying (DAC 7541)
Linearity	:	+/- ½ bit.
Output Drive	:	+/- 5 mA max.
Settling Time	:	5 microseconds.

General Specifications:

Power Consumption	:	+5 V :	typ. 700 mA, max. 1A.
		+12 V :	typ. 140 mA, max. 200 mA.
		-12 V :	typ. 14 mA, max. 20 mA.
I/O Connector	:	20 pin flat cable connector for all Analog/Digital I/O ports.	
I/O Base Address	:	Requires 16 consecutive address locations. Base address is definable by the DIP switches for address lines A9 – A4.	

Specifications used in Experimental work: 16 Single-ended Analog input channels, bipolar +/-10 V, -5 V internal reference.

Appendix-C

Program for Real Time closed loop control

```
/* Program used for closed loop control of Synchronous Link Converter */
#include<stdio.h>
#include<conio.h>
#include<time.h>
#include<dos.h>
#include<math.h>
#include BASE_ADDRESS ox300H
void main ()
{       float kp = 0.1, ki = 2.5, im, vl, vdc, vdc_ref = 100.0, err, er0, pi, Ls = 7.146;
        int check = 0, u = 0, val = 0, vl2 = 2047, hi = 159, lo = 240, lo1 = 0, muxscan,
        trigger, ch1, ch1, ch0;
        double T = 0.000002;
        while (1)
        {       muxscan = 0;
                trigger = 0;
                outportb (BASE_ADDRESS + 2,muxscan);
                outportb (BASE_ADDRESS + 0,trigger);
                while ( 1 )
                {       u = inportb (BASE_ADDRESS + 8);
                        check = u;
                        check & = 0x80;
                        if (!check)
                        break;
                }
                ch0 = inportb (BASE_ADDRESS+0);
                ch1 = ch0 >> 4;
                ch2 = inportb (BASE_ADDRESS+1);
```

```
            val = ((ch2&0xff) * 16 + ch1);
            vdc = (val-2047) * 200.0/2047;
            err = vdc_ref – vdc;
            if ((err < 0.1) && (err > -0.1))
            {       err = 0.0;
            }
            pi = pi + kp * (err – er0) + ki * err * T;
            er0 = err;
            im = pi;
            vl = im * Ls;
            if (vl > 38.0)
            {       vl = 38.0;
                    pi = 5.25;
            }
            if (vl < -38.0)
            {       vl = -38.0;
                    pi = -5.25;
            }
            vl2 = ((vl * 2047) / 38) + 2048;
            lo1 = vl2 % 16;
            lo = lo1 << 4;
            hi = vl2 / 16;
            outportb (BASE_ADDRESS + 4,lo);
            outportb (BASE_ADDRESS + 5,hi);
        }
}
```